Instruction Manual

Tektronix

TMS 109A
Socket 7 Microprocessor Support

071-0497-01

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Connect and Disconnect Properly. Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Disconnect the probe input and the probe ground from the circuit under test before disconnecting the probe from the measurement instrument.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

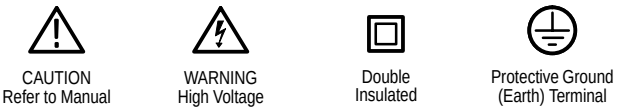
Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 109A Socket 7 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 109A Socket 7 support was purchased, you will only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

NOTE. *The disassembly software is optimized to decode instruction streams and bus activities from Intel microprocessors and AMD-K6-2 therefore, the disassembler may not support unique characteristics of other manufacturers. However, you can reliably conduct timing analysis of nonIntel Socket 7 processors. Consult your Tektronix field office for future enhancements.*

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that decodes bus cycles into instruction mnemonics and cycle types.
- A pound sign (#) following a signal name indicates an active low signal.
- The phrase “information on basic operations” refers to your online help.

Contacting Tektronix

Product Support	For questions about using Tektronix measurement products, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Tektronix offers extended warranty and calibration programs as options on many products. Contact your local Tektronix distributor or sales office. For a listing of worldwide service centers, visit our web site.
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000 USA
Website	Tektronix.com

Getting Started

Getting Started

This chapter contains information on the TMS 109A Socket 7 microprocessor support package:

- How to configure the probe adapter
- How to connect to the system under test
- How to apply power to and remove power from the probe adapter

Support Package Description

The TMS 109A Socket 7 microprocessor support package disassembles data from systems that are based on the Intel Pentium, low-power embedded Pentium with MMX technology, AMD-K6-2 and Socket 7 microprocessor devices. The support runs on a compatible Tektronix logic analyzer equipped with a 136-channel module.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts List* chapter.

To use this support efficiently, you must have the items listed in the information on basic operations (in the online help) and the following items:

- *Pentium Processors Family Developer's Manual, Intel 1997(p/n to be updated)*
- *AMD-K6-2 Processor, Data Sheet, AMD, 1999*

Information on basic operations is also in your online help.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 109A Socket 7 support package, the Tektronix logic analyzer must be equipped with a 136-channel module at a minimum.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 109A Socket 7 microprocessor support.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your system under test.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other Socket 7 support requirements and restrictions.

System Clock Rate. The TMS 109A Socket 7 support can acquire data from the Socket 7 microprocessors at bus speeds of up to 100 MHz; the tested clock speed is 100 MHz. This specification is valid at the time this manual was printed. Contact your Tektronix sales representative for current information on the fastest devices supported.

System Under Test Power. Whenever the system under test is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* on page 1–13 for information on how to remove power from the probe adapter.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Cache Invalidation Cycles. Cache Invalidation addresses are not acquired.

Bus Hold Cycles. Bus Hold cycles are not acquired while the RESET signal is active.

AHOLD Signal. If the AHOLD signal is active (high) during a Writeback cycle (a four cycle Burst Write), the acquired address is undefined.

Burst Cycles. The Socket 7 microprocessor expects the memory system to increment addresses during a Burst cycle. When viewing disassembled data, the disassembler synthesizes the addresses. When viewing state data, the addresses appear to be identical.

Probe Mode Cycles. Probe Mode cycles are not identified.

Directory Table and Descriptor Table Reads and Writes. These reads and writes are not disassembled.

Bus Anomalies. Some combinations of instructions and operating modes of the microprocessor can cause additional cycles to be fetched. This behavior is unpredictable, not documented, and can cause the disassembler to operate incorrectly with fetched cycles. This is most likely to occur during Floating Point operations.

AMD-K6-2 processor has a out-of-order fetch mechanism. For fetches, AMD always loads 32 bytes, starting from the most significant octabyte (octet) in the block. For example these addresses 00, 08, 10, and18 would be fetched in this order 18, 10, 08, and 00. Regardless of what the critical word is or if the cache is enabled. For the disassembler to work properly it needs these 32 byte fetch blocks or the disassembly will be incorrect.

Nonintrusive Acquisition. The Socket 7 microprocessor support will not intercept, modify, or present signals back to the system under test.

Functionality Not Supported

Reads/Writes. The TMS 109A Socket 7 support package does not interpret directory or descriptor tables for reads/writes. When long jumps and calls are executed you may need to supply a code-segment size (see page 2–18), and the first opcode byte using the Mark Opcode function (see page 2–25).

Configuring the Probe Adapter

There are five jumpers on the probe adapter. Table 1–1 lists the jumper positions and functions.

Table 1–1: Jumper positions and function

Probe adapter	Position	Function
J240 MFG_TEST	1–2	When the processor extends the clock speed to below 40 MHz, the jumpered pins 1-2 turn the phased lock loop into a buffer that disables the phased lock loop signal.
	OPEN	Default, phased look loop signal enabled
J250 CLK	1–2	Extends the Socket 7 microprocessor system speed between 40–150 MHz
	2–3	Extends the Socket 7 microprocessor system speed between 20–75 MHz
J900 Proc Sel	1–2	Supports microprocessors that do not have the D/P# pin.
	2–3	Supports microprocessors that have the D/P# pin.
J910 D/P#	1–2	Acquires the D/P# signal from pin AE35 of the socket being probed.
	OPEN	Acquires the D/P# signal from an external source. If this jumper is left open, you must route the D/P# signal to pin 1 of this jumper from an external source. This allows you to probe your system from the Dual socket as long as the D/P# signal is accessible on the system board. Ensure that the jumper J900 is in position 2–3 before routing the D/P# signal to pin 1 of J910.
J920 Tracking	1–2	Enables tracking of burst and pipelined cycles while BOFF# and HLDA are asserted
	2–3	Disables tracking of burst and pipelined cycles while BOFF# and HLDA are asserted. This setting can be used if an external master's signal timing is different from that of the P54C.
J921 SYNTH	1–2	Enable Address Synthesis (A(2:0) are derived from BE(7:0)#)
	2–3	Disable Address Synthesis (A(2:0)=0)

MFG_TEST Jumper

To acquire data at frequencies below 40 MHz on the probe adapter, short the two pins on J240. This disables the phased lock loop signal to all clocked components. Figure 1–1 shows the location of J240 on the probe adapter.

CLK Jumper

The CLK jumper (J250 on the probe adapter) should be placed in the 40–150 MHz position to acquire data from a system running at or faster than 45 MHz. The jumper should be placed in the 20–75 MHz position to acquire data from a system running slower than 45 MHz. Figure 1–1 shows the location of J250 on the probe adapter.

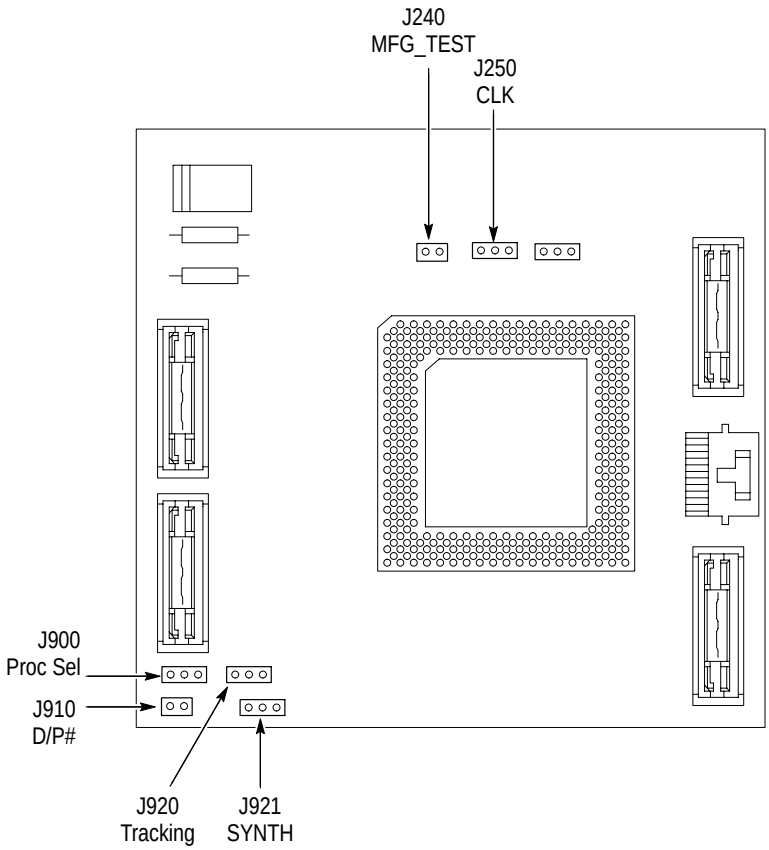


Figure 1–1: Jumper locations on the probe adapter

Processor Selection Jumper

Place the Processor Selection jumper, J900, in the 1–2 position to support microprocessors that do not have the D/P# pin.

Place the Processor Selection jumper in the 2–3 position to support microprocessors that have the D/P#. Figure 1–1 shows the location of J900 on the probe adapter.

D/P# Signal Jumper

When the D/P# signal jumper J910 on the probe adapter is in the 1– 2 position, the D/P# signal is acquired from pin AE35 of the socket being probed. Figure 1–1 shows the location of J910 on the probe adapter.

When the jumper is open (not connected), the Socket 7 support acquires the D/P# signal from an external source, and you will have to route the D/P# signal to pin 1 of this jumper externally. This allows you to probe your system from the dual socket as long as the D/P# signal is accessible on the system under test.

Tracking Jumper

The Tracking jumper J920 on the probe adapter (see Figure 1–1) does not need to be moved from the default position (pins 1–2 connected).

The only time this jumper should be moved is when the tracking circuitry malfunctions. An indication of such a malfunction is when you see activity on the bus during a BOFF or HLDA cycle that is uncharacteristic of the Socket 7 microprocessor. When the jumper is in the 2–3 position, the circuitry on the probe adapter does not track BOFF and HLDA cycles. A data sample will show that such a cycle occurred, but it will not contain meaningful information.

Address Synthesis Jumper

When the Address Synthesis jumper (J921 on the probe adapter) is in position 1–2, A(2:0) is derived from the BE(7:0)# signals and stored in the acquisition memory with the rest of the address.

When the jumper is in position 2–3, it disables address synthesis, A(2:0)=0. Figure 1–1 shows the location of J921 on the probe adapter.

Connecting to a System Under Test

Before you connect to the system under test, you must connect the probes to the module. Your system under test must also have a minimum amount of clearance surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

Connect the P6434 Probes to the Probe Adapter

To connect the logic analyzer to a system under test using a probe adapter, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage to the microprocessor, the probe adapter, the probes, and the module, handle in a static-free environment. Static discharge can damage all the above components.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.

3. Connect the P6434 probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

CAUTION. *To prevent damage to the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe. Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter.*

4. Position the probe tip perpendicular to the mating connector and gently connect the probe (see Figure 1–2).

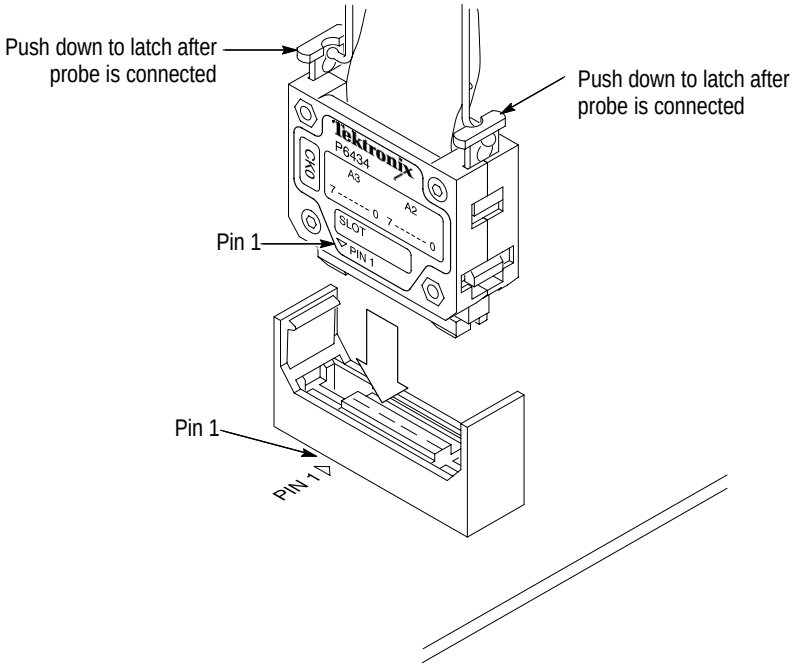


Figure 1–2: Connecting a probe to the probe adapter

5. When connected, push down the latch releases on the probe to set the latch.

Remove the Microprocessor

6. Follow the procedure from the Socket 7 microprocessor vendor to remove the microprocessor from the socket on your system under test.

Choose a Protective Socket

7. Choose the correct protective socket.

Choose the 321-pin or 296-pin protective socket depending on the processor pinout (see Figure 1–3).

NOTE. *Use one protective socket at a time. Do not install a protective socket without removing all existing sockets from the system under test and from the bottom of the probe adapter assembly.*

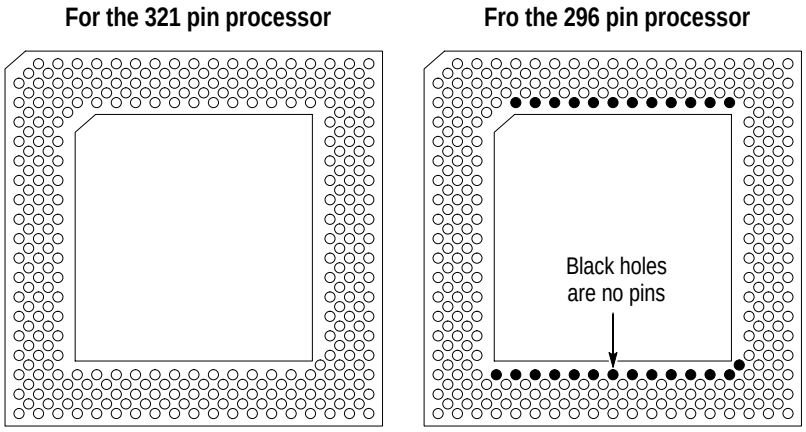


Figure 1–3: Protective sockets

8. Align the A3 pin indicator on the protective socket with A3 pin of the socket on your system under test.

9. Insert the protective socket into the system under test as shown in Figure 1–4.

10. Align the A3 pin indicator on the probe adapter with the A3 pin indicator on the installed protective socket.

Insert Probe Adapter

11. Insert the probe adapter into the installed protective socket as shown in Figure 1–4.

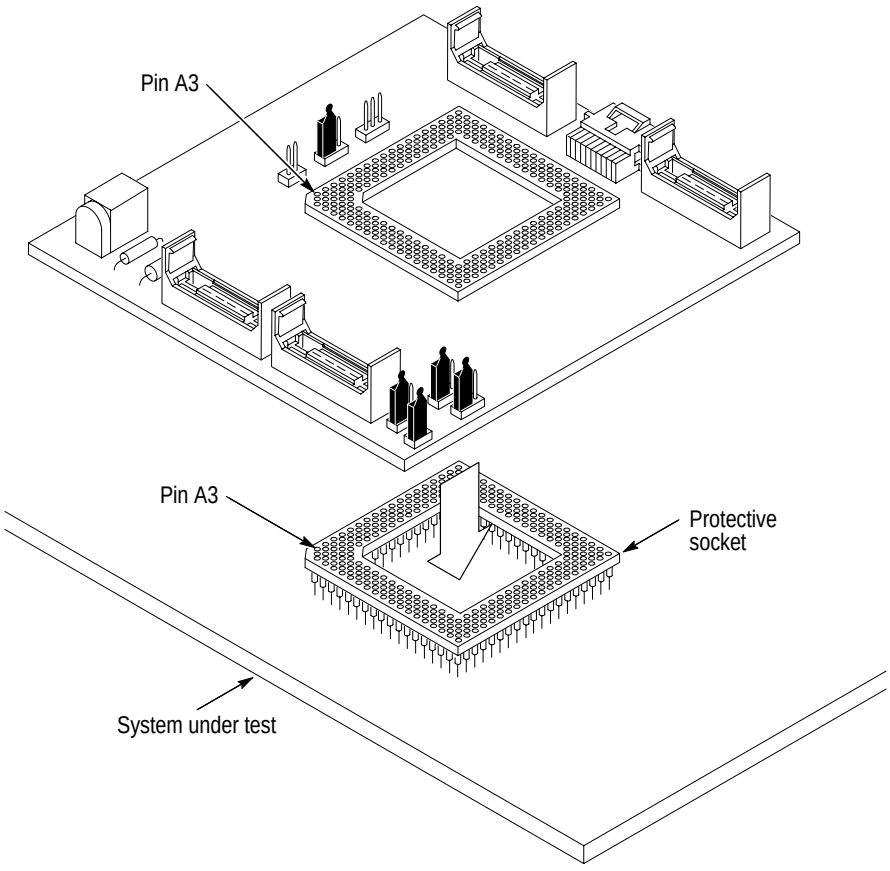


Figure 1–4: Placing the socket and probe adapter onto the system under test

CAUTION. *To prevent permanent damage to the microprocessor once power is applied, correctly place the microprocessor into the probe adapter.*

Insert Microprocessor in the Probe Adapter

12. Insert the microprocessor into the probe adapter as shown in Figure 1–5.

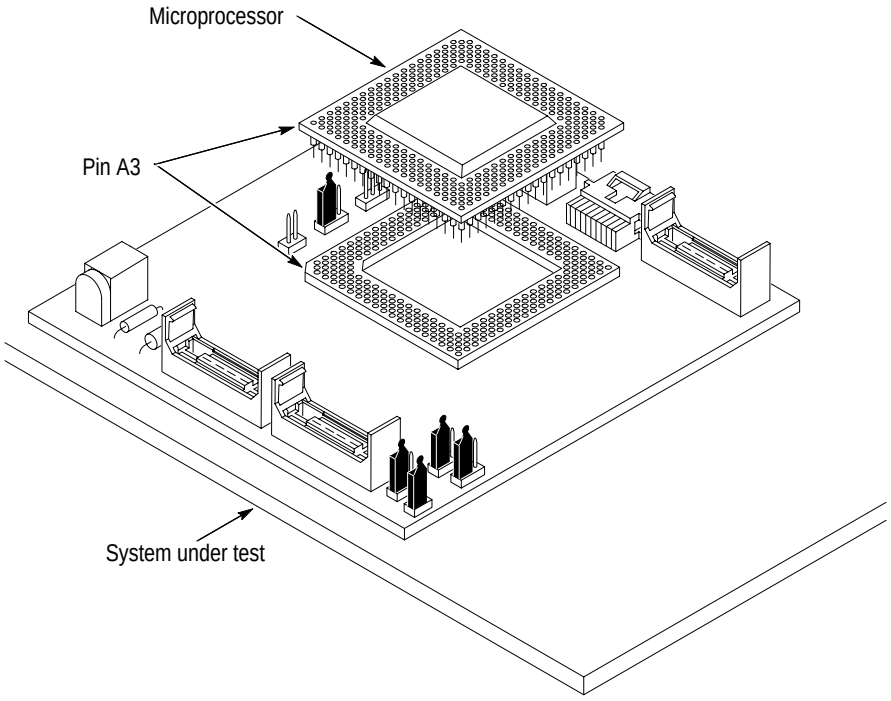


Figure 1–5: Inserting a microprocessor into the probe adapter

13. Apply forced air cooling across the probe adapter to keep the components on the probe adapter cool.

Alternate Connections

NOTE*. Refer to the Intel document* ITP700 Port Users Guide *for more information on the ITP interface.*

ITP

The Socket 7 probe adapter provides an ITP square-pin header (J580) to connect to the In-Target Probing (ITP) debugging hardware on the probe adapter as shown in Figure 1–6 on page 1–12. Table 1–2 lists the signals on the connector (J580). The ITP debugging hardware is not included with this TMS 109A Socket 7 hardware support package. Contact your microprocessor vendor for information on how to obtain the ITP debugging hardware.

***NOTE**. The ITP connection is implemented as a point-to-point connection. As such, it cannot be used in a loopthrough mode for programming other Socket 7 modules.*

Table 1–2 lists the pin-to-signal assignments of the In-Target Probe (ITP) connector J580 on the probe adapter**.**

Table 1–2: ITP (J580) signal Information

Pin number	Signal name
1	B_INIT
2	DBRESET
3	B_RESET
4	GND
5	–
6	+3.3 V
7	R_S#
8	GND
9	–
10	GND
11	PRDY
12	TDI
13	TDO
14	TMS
15	GND
16	TCK
17	GND
18	TRST#
19	–
20	–

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

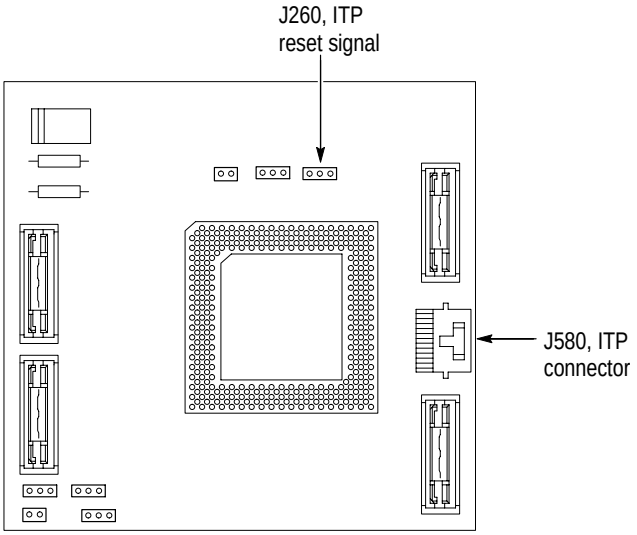


Figure 1–6: ITP and system reset pin locations on the probe adapter

Optional System Reset. The ITP circuitry on the Interposer board does not allow external ITP debugging hardware to induce a system reset through the DBRESET# signal on the ITP connector. If you need to enable this feature, you must provide the connection to your system under test. Table 1–3 lists the signals on J260 and Figure 1–6 shows the location.

Table 1–3: J260 jumper pin assignments

Jumper pin number	Socket 7 signal name
1	OC_DBRESET# (Open Collector, active low version of DBRESET)
2	NC
3	DBRESET

The probe adapter contains pins that allow you to connect the DBRESET (or the active low, open collector version OC_DBRESET#) signal to your system under test. Table 1–3 shows the pins and signals you can connect to on J260 on the probe adapter.

When using these signals, you need to make sure that the system under test is not driving the OC_DBRESET# or DBRESET signal.

Check that the R/S#, TDI, TMS, TCLK, and TRST# signals are not driven. If this is not possible, you may clip these five pins on one of the sacrificial sockets

provided with the probe adapter. Inserting this modified socket into your system socket will isolate these signals on the probe adapter for use by the ITP cable.

Applying and Removing Power

A power supply for the Socket 7 probe adapter is included with the support. The power supply provides +5 volts power to the probe adapter. The center connector of the power jack connects to Vcc.

NOTE. *Whenever the system under test is powered off, be sure to remove power from the probe adapter.*

To apply power to the Socket 7 probe adapter and system under test, follow these steps:

CAUTION. *To prevent possible permanent damage to the probe adapter and Socket 7 microprocessor., use the +5 V power supply provided by Tektronix. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–7 shows the location of the jack on the probe adapter.

CAUTION. *To prevent possible permanent damage to the Socket 7 microprocessor and system under test, apply power to the probe adapter before applying power to your system under.*

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the system under test.

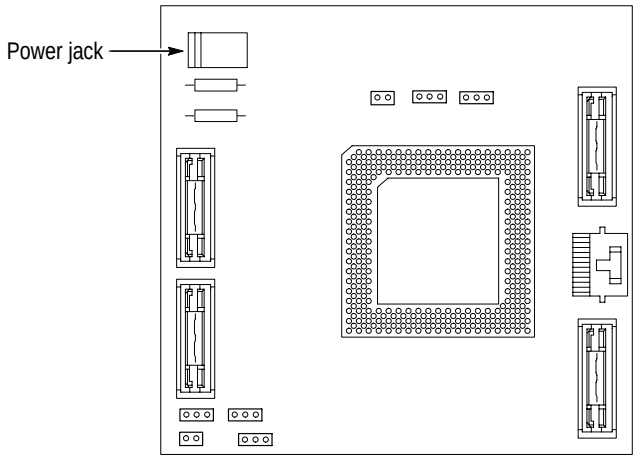


Figure 1–7: Power jack location on the probe adapter

Channel Assignments

Channel assignments shown in Tables 1–4 through 1–10 use the following conventions:

- A pound sign (#) following a signal name indicates an active low signal.
- All signals are required by the support unless indicated otherwise.
- An equals sign (=) following a signal name indicates that it is double probed.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).

The channel group assignment tables for disassembly and Timing are Address, Data, Data_Lo, Control, DataSize, Cache, and Misc.

Table 1–4 lists the probe section and channel assignments for the Address group and the microprocessor signal for each channel connect. By default the Address channel group assignments are displayed in hexadecimal.

Table 1–4: Address channel group assignments

Bit order	Section:channel	Socket 7 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28

Table 1–4: Address channel group assignments (Cont.)

Bit order	Section:channel	Socket 7 signal name
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2_D
1	A0:1	A1_D
0	A0:0	A0_D

Table 1–5 lists the probe section and channel assignments for the Data group and the microprocessor signal for each channel connect. By default the Data channel group assignments are displayed in hexadecimal.

Table 1–5: Data channel group assignments

Bit order	Section:channel	Socket 7 signal name
31	E3:7	D63
30	E3:6	D62
29	E3:5	D61
28	E3:4	D60
27	E3:3	D59
26	E3:2	D58
25	E3:1	D57
24	E3:0	D56
23	E2:7	D55
22	E2:6	D54
21	E2:5	D53
20	E2:4	D52
19	E2:3	D51
18	E2:2	D50
17	E2:1	D49
16	E2:0	D48
15	E1:7	D47
14	E1:6	D46
13	E1:5	D45
12	E1:4	D44
11	E1:3	D43
10	E1:2	D42
9	E1:1	D41
8	E1:0	D40
7	E0:7	D39
6	E0:6	D38
5	E0:5	D37
4	E0:4	D36
3	E0:3	D35
2	E0:2	D34
1	E0:1	D33
0	E0:0	D32

Table 1–6 lists the probe section and channel assignments for the Data_Lo group and the microprocessor signal for each channel connect. By default the Data_Lo channel group assignments are displayed in hexadecimal.

Table 1–6: Data_Lo channel group assignments

Bit order	Section:channel	Socket 7 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3

Table 1–6: Data_Lo channel group assignments (Cont.)

Bit order	Section:channel	Socket 7 signal name
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 1–7 lists the probe section and channel assignments for the Control group and the microprocessor signal for each channel connect. The symbol table file name is SOCKET7_Ctrl. By default the Control channel group assignments are displayed as symbols.

Table 1–7: Control channel group assignments

Bit order	Section:channel	Socket 7 signal name
14	C0:7	D/P#
13	C3:0	INIT
12	C2:0	RESET_L
11	C3:6	PRDY
10	C3:5	BUSCHK#
9	C2:5	SMIACT#
8	C2:6	LOCK#
7	C0:6	SCYC
6	CLK2	LAST_D
5	C0:4	AHOLD
4	C2:2	HLDA
3	C2:1	BOFF#
2	C2:7	M/IO#
1	C3:7	D/C#
0	C3:3	LAST_D

 # Indicates the channel is asserted low.

Table 1–8 lists the probe section and channel assignments for the Data Size group and the microprocessor signal for each channel connect. By default the Data Size channel group assignments are not displayed.

Table 1–8: Data Size channel group assignments

Bit order	Section:channel	Socket 7 signal name
7	C1:7	BE7#
6	C1:6	BE6#
5	C1:5	BE5#
4	C1:4	BE4#
3	C1:3	BE3#
2	C1:2	BE2#
1	C1:1	BE1#
0	C0:0	BE0#

 # Indicates the channel is asserted LOW.

Table 1–9 lists the probe section and channel assignments for the Cache group and the microprocessor signal for each channel connect. By default the Cache channel group assignments are not displayed.

Table 1–9: Cache channel group assignments

Bit order	Section:channel	Socket 7 signal name
	C0:5	CACHE#

 # Indicates the channel is asserted LOW.

Table 1–10 lists the probe section and channel assignments for the Misc group and the microprocessor signal for each channel connect. By default the Misc channel group assignments are not displayed.

Table 1–10: Misc channel group assignments

Bit order	Section:channel	Socket 7 signal name
3	CLK3	CLK
2	C2:3	ADS#
1	C3:2	NA#

Table 1–10: Misc channel group assignments (Cont.)

Bit order	Section:channel	Socket 7 signal name
0	C3:4	BRDY#

 # Indicates the channel is asserted LOW.

Table 1–11 lists the probe section and channel assignments for the clock probes and the Socket 7 signal to which each channel connects.

Table 1–11: Clock channel group assignments

Section:channel	Socket 7 signal name	Description
CLK:0	DVALID_D	
CLK:1	PIPE_D	
CLK:2	LAST_D	
CLK:3	CLK	
C2:0	RESET_L	
C2:1	BOFF#	
C2:2	HLDA	
C2:3	ADS#	
QUAL:0	Not Used	
QUAL:1	Not Used	
QUAL:2	Not Used	
QUAL:3	Not Used	

 # Indicates the channel is asserted low.

Acquisition Setup. The support will affect the logic analyzer setup menus and submenus by modifying existing fields and adding micro-specific fields.

The TMS 109A Socket 7 microprocessor support will add the selections SOCKET7_ to the Load Support Package dialog box, located under the File pulldown menu. The SOCKET7_T supports timing.

Once the TMS 109A Socket 7 support has been loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

Table 1–12 lists channel groups not required for clocking and disassembly.

Table 1–12: Signals not required for clocking or disassembly

Signal name	TLA700 Channel
NA#	C3:2
BRDY#	C3:4
CACHE#	C0:5

 # Indicates the channel is asserted low.

Table 1–13 lists signals on the probe adapter but not acquired.

Table 1–13: Signals on the probe adapter but not acquired

Signal name	AUX J580 Pin number
TDI	12
TDO	13
TMS	14
TCK	16
TRST#	18
INIT	1
R/S#	7
PRDY	11

 # Indicates the channel is asserted low.

Table 1–14 lists signals not connected to probe adapter.

Table 1–14: Signals not connected to probe adapter

Signal name	AUX J1700 Pin number
A20M#	AK08
AP	AK02
BREQ	AJ01
EWBE#	W03
IERR#	P04
FRCMC#	Y35

Table 1–14: Signals not connected to probe adapter (Cont.)

Signal name	AUX J1700 Pin number
ADSC#	AM02
BRDYC#	Y03
KEN#	W05

 # Indicates the channel is asserted low.

Channel Qual 0:3 is not attached to the probe adapter by default. You may connect this channel to other signals of interest.

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 1–15 through 1–17 show the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin 1 is located at the top left, and pin 2 is located directly below it. Pin 20 is located on the bottom right, and pin 21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin-1 is located at the top left, and pin 3 is located directly below it. Pin 2 is located on the top right, and pin 4 is located directly below it (see Figure 1–8).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

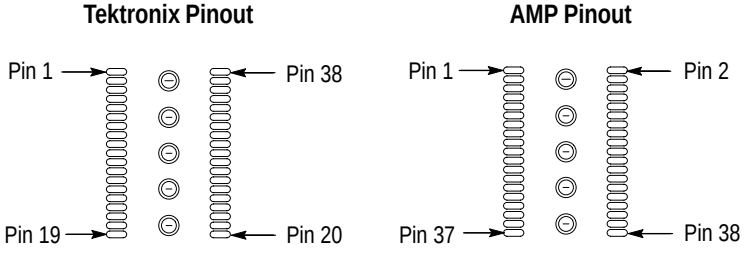


Figure 1–8: Pin assignments for a Mictor connector (component side)

Table 1–15: CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	Socket 7 signal name	Socket 7 pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	CLOCK:0	DVALID_D	DERIVED
4	7	A3:7	A31	AJ-33
5	9	A3:6	A30	AM-36
6	11	A3:5	A29	AK-34
7	13	A3:4	A28	AK-36
8	15	A3:3	A27	AG-33
9	17	A3:2	A26	AH-34
10	19	A3:1	A25	AJ-35
11	21	A3:0	A24	AG-35
12	23	A2:7	A23	AE-33
13	25	A2:6	A22	AH-36
14	27	A2:5	A21	AF-34
15	29	A2:4	A20	AL-21
16	31	A2:3	A19	AK-22
17	33	A2:2	A18	AL-23
18	35	A2:1	A17	AK-24
19	37	A2:0	A16	AL-25
20	38	A0:0	A0_D	DERIVED
21	36	A0:1	A1_D	DERIVED
22	34	A0:2	A2_D	DERIVED
23	32	A0:3	A3	AL-35
24	30	A0:4	A4	AM-34
25	28	A0:5	A5	AK-32
26	26	A0:6	A6	AN-33
27	24	A0:7	A7	AL-33
28	22	A1:0	A8	AM-32
29	20	A1:1	A9	AK-30
30	18	A1:2	A10	AN-31
31	16	A1:3	A11	AL-31
32	14	A1:4	A12	AL-29
33	12	A1:5	A13	AK-28
34	10	A1:6	A14	AL-27
35	8	A1:7	A15	AK-26

Table 1–15: CPU to Mictor connections for Mictor A pins (Cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	Socket 7 signal name	Socket 7 pin number
36	6	CLOCK:1	PIPE_D	DERIVED
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND
44	44	GND	GND	GND

Table 1–16: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor D pin number	LA channel	Socket 7 signal name	Socket 7 pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	NC	NC	NC
4	7	D3:7	D31	C-17
5	9	D3:6	D30	D-20
6	11	D3:5	D29	C-19
7	13	D3:4	D28	D-22
8	15	D3:3	D27	C-21
9	17	D3:2	D26	D-24
10	19	D3:1	D25	C-23
11	21	D3:0	D24	C-27
12	23	D2:7	D23	D-26
13	25	D2:6	D22	A-31
14	27	D2:5	D21	C-29
15	29	D2:4	D20	B-30
16	31	D2:3	D19	D-28
17	33	D2:2	D18	A-33
18	35	D2:1	D17	C-31
19	37	D2:0	D16	B-32
20	38	D0:0	D0	K-34

Table 1–16: CPU to Mictor connections for Mictor D pins (Cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	LA channel	Socket 7 signal name	Socket 7 pin number
21	36	D0:1	D1	G-35
22	34	D0:2	D2	J-35
23	32	D0:3	D3	G-33
24	30	D0:4	D4	F-36
25	28	D0:5	D5	F-34
26	26	D0:6	D6	E-35
27	24	D0:7	D7	E-33
28	22	D1:0	D8	D-34
29	20	D1:1	D9	C-37
30	18	D1:2	D10	C-35
31	16	D1:3	D11	B-36
32	14	D1:4	D12	D-32
33	12	D1:5	D13	B-34
34	10	D1:6	D14	C-33
35	8	D1:7	D15	A-35
36	6	CLOCK:2	LAST_D	DERIVED
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND
44	44	GND	GND	GND

Table 1–17: CPU to Mictor connections for Mictor E pins

Tektronix Mictor E pin number	AMP Mictor E pin number	LA channel	Socket 7 signal name	Socket 7 pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	QUAL:3	NC	NC
4	7	E3:7	D63	N-03
5	9	E3:6	D62	M-04

Table 1–17: CPU to Mictor connections for Mictor E pins (Cont.)

Tektronix Mictor E pin number	AMP Mictor E pin number	LA channel	Socket 7 signal name	Socket 7 pin number
6	11	E3:5	D61	L-03
7	13	E3:4	D60	L-05
8	15	E3:3	D59	K-04
9	17	E3:2	D58	J-05
10	19	E3:1	D57	J-03
11	21	E3:0	D56	H-04
12	23	E2:7	D55	G-03
13	25	E2:6	D54	E-01
14	27	E2:5	D53	G-05
15	29	E2:4	D52	E-03
16	31	E2:3	D51	F-04
17	33	E2:2	D50	D-02
18	35	E2:1	D49	E-05
19	37	E2:0	D48	D-04
20	38	E0:0	D32	C-15
21	36	E0:1	D33	D-16
22	34	E0:2	D34	C-13
23	32	E0:3	D35	D-14
24	30	E0:4	D36	C-11
25	28	E0:5	D37	D-12
26	26	E0:6	D38	C-09
27	24	E0:7	D39	D-10
28	22	E1:0	D40	D-08
29	20	E1:1	D41	A-05
30	18	E1:2	D42	E-09
31	16	E1:3	D43	B-04
32	14	E1:4	D44	D-06
33	12	E1:5	D45	C-05
34	10	E1:6	D46	E-07
35	8	E1:7	D47	C-03
36	6	QUAL:2	NC	NC
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND

Table 1–17: CPU to Mictor connections for Mictor E pins (Cont.)

Tektronix Mictor E pin number	AMP Mictor E pin number	LA channel	Socket 7 signal name	Socket 7 pin number
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND

Table 1–18: CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor C pin number	LA channel	Socket 7 signal name	Socket 7 pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	CLOCK:3	CLK	AK-18
4	7	C3:7	D/C#	AK-04
5	9	C3:6	PRDY	AC-05
6	11	C3:5	BUSCHK#	AL-07
7	13	C3:4	BRDY#	DERIVED
8	15	C3:3	W/R#	DERIVED
9	17	C3:2	NA#	Y-05
10	19	C3:1	BRDY#=	X-04
11	21	C3:0	INIT	AA-33
12	23	C2:7	M/IO#	T-04
13	25	C2:6	LOCK#	AH-04
14	27	C2:5	SMIACT#	AG-03
15	29	C2:4	W/R#=	AM-06
16	31	C2:3	ADS#	DERIVED
17	33	C2:2	HLDA	DERIVED
18	35	C2:1	BOFF#	DERIVED
19	37	C2:0	RESET_L	DERIVED
20	38	C0:0	RESET_L=	AK-20
21	36	C0:1	BOFF#=	Z-04
22	34	C0:2	HLDA=	AJ-3
23	32	C0:3	ADS#=	AJ-05
24	30	C0:4	AHOLD	V-04
25	28	C0:5	CACHE#	DERIVED
26	26	C0:6	SCYS	AL-17

Table 1–18: CPU to Mictor connections for Mictor C pins (Cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA channel	Socket 7 signal name	Socket 7 pin number
27	24	C0:7	D/P#	DERIVED
28	22	C1:0	BE0#	AL-09
29	20	C1:1	BE1#	AK-10
30	18	C1:2	BE2#	AL-11
31	16	C1:3	BE3#	AK-12
32	14	C1:4	BE4#	AL-13
33	12	C1:5	BE5#	AK-14
34	10	C1:6	BE6#	AL-15
35	8	C1:7	BE7#	AK-16
36	6	NC	–	NC
37	4	NC	GND	GND
38	2	NC	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND

 # Indicates the channel is asserted low.

= Indicates double probing

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 109A Socket 7 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the Socket 7 support are Address, Data, Data_Lo, Control, DataSize, Cache, and Misc.

Clocking Options

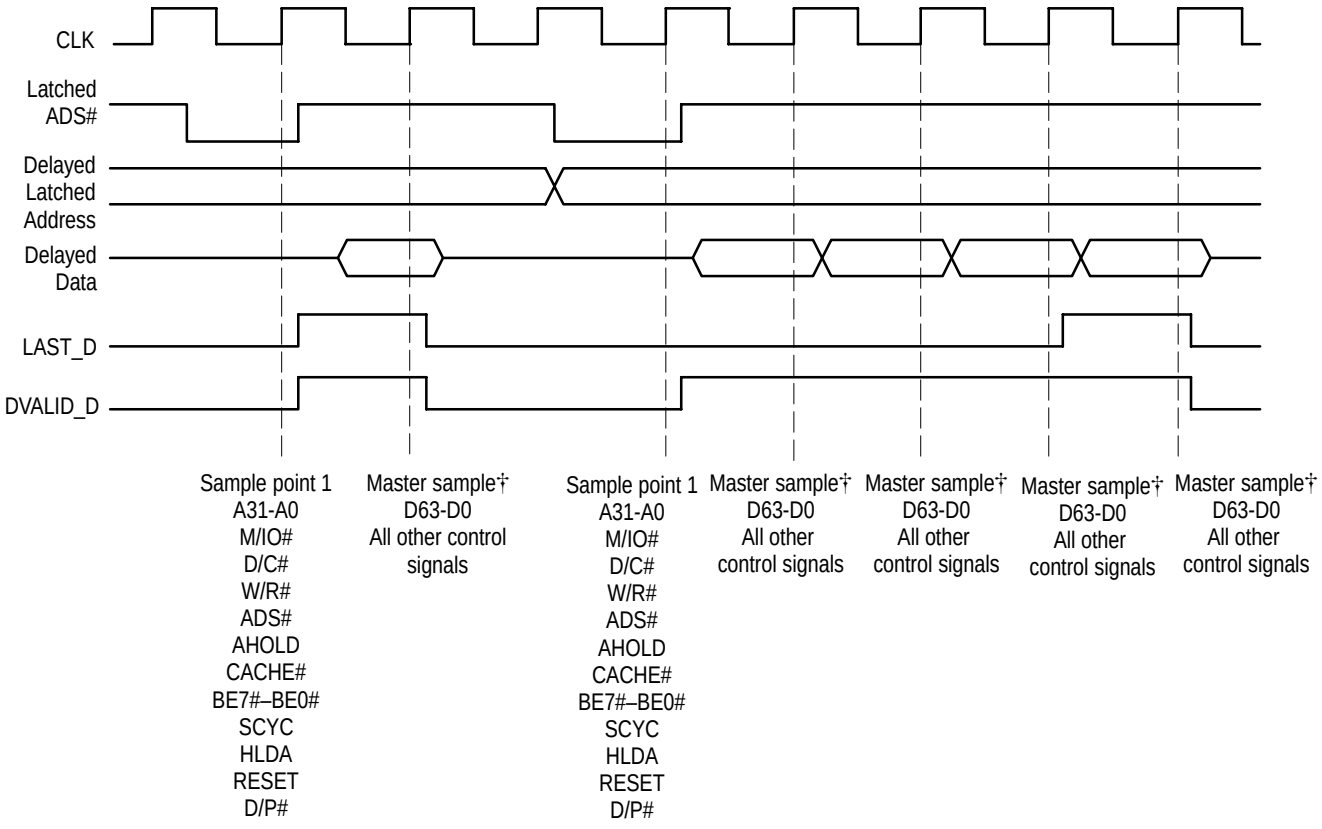
Custom Clocking

A special clocking program is loaded to the module every time you load the SOCKET7_ support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the Socket 7 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 2–1 shows two typical bus cycles: a single cycle transfer followed by a burst transfer. The ADS#, Address and Data signal forms are delayed by two CLK cycles. This diagram also shows the timing relationships of LAST_D and DVALID_D, the signals synthesized by sequential logic in the PALs.



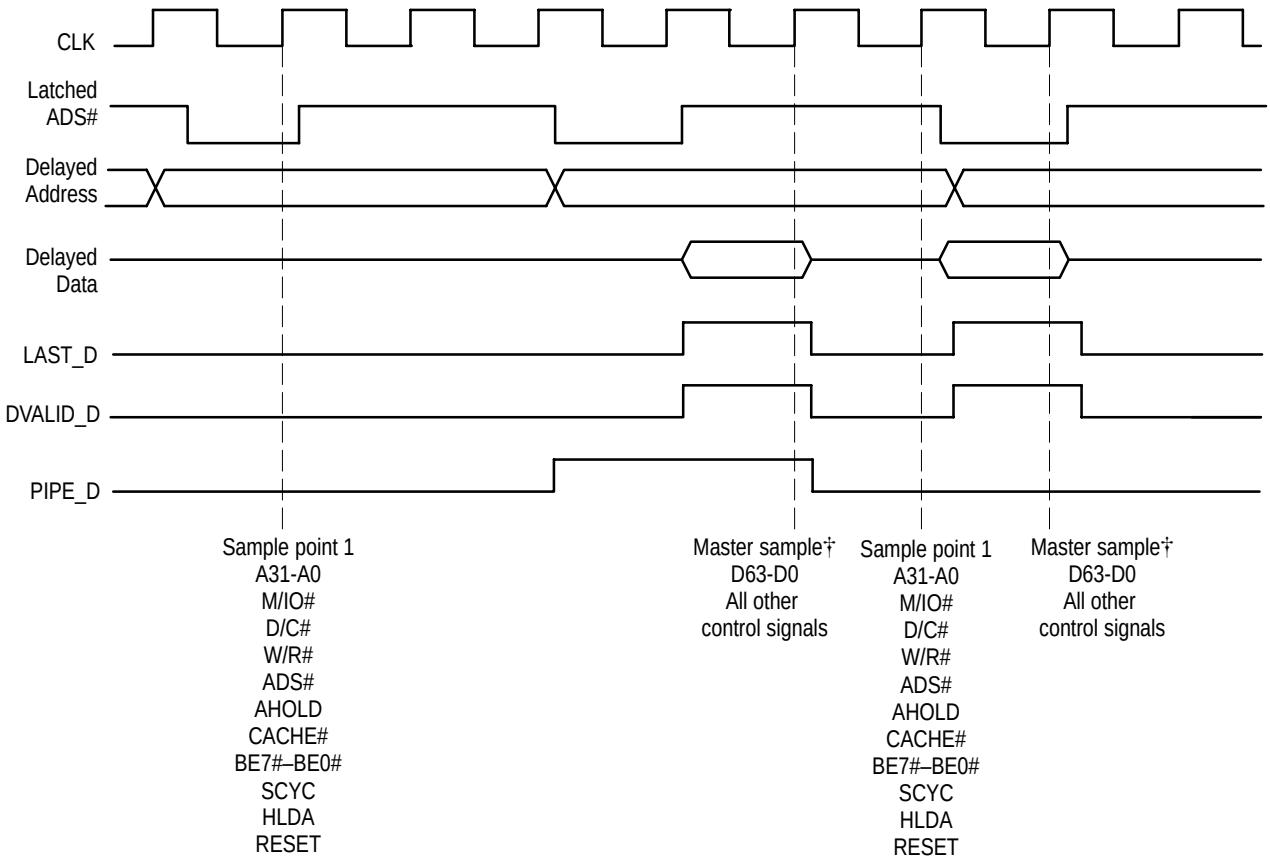
†Channels not set up in a channel group by the TMS 109A Socket 7 software are logged with the Master sample.

Figure 2–1: Nonpipelined single and Burst Transfer cycles

Relative to real time, nondelayed Socket 7 microprocessor signals, the first sample point in a cycle occurs two clocks after the ADS# signal is asserted. The second (and subsequent, if the cycle is a burst) sample point occurs two clocks after the BRDY# or BRDYC# signal.

Figure 2–2 shows a single cycle transfer pipelined into another single cycle transfer. The ADS#, Address and Data signal forms are delayed by two CLK cycles. This diagram also shows the timing relationships of D_LAST,

DVALID_D, and PIPE_D, which are the signals synthesized by sequential logic in the PALs.



†Channels not set up in a channel group by the TMS 109A Socket 7 software are logged with the Master sample.

Figure 2–2: Pipelined cycles

With relationship to real-time, nondelayed, Socket 7 microprocessor signals, the first sample point in a cycle occurs two clocks after the ADS# signal is asserted. When the ADS# signal is asserted again to pipeline a second cycle into the first, the first sample point for that second cycle occurs three clocks after the last BRDY# or BRDYC# signal is returned from the first outstanding cycle.

ClockingOptions

The clocking algorithm for the Socket 7 microprocessor has two variations: Alternate Bus Master Cycles Excluded and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles driven by the microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

Alternate Bus Master Cycles Included. All bus cycles, including alternate bus master cycles and backoff cycles, are logged in.

When the HLDA signal is high, the microprocessor has given up the bus to an alternate device. The design of the Socket 7 microprocessor system affects what data will be logged in. The module only samples the data at the pins of the microprocessor. To properly log in bus activity, any buffers between the microprocessor and the alternate bus master must be enabled and pointing at the Socket 7 microprocessor.

There are three possible Socket 7 microprocessor system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the alternate bus master drives the same control lines as the Socket 7 microprocessor, and the Socket 7 microprocessor sees these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.
- If none of the control lines are driven or if the Socket 7 microprocessor can not see them, the module will still clock in an alternate bus master cycle. The information on the bus, one clock prior to the HLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HLDA signal goes low, the address that gets logged in will be the next address, not the address that occurred one clock before the HLDA signal went low.
- If some of the Socket 7 microprocessor control lines are visible (but not all), the module logs in the signals it determines are valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the next address will be logged instead of the previously saved address.

When the BOFF# signal goes low (active), a backoff cycle has been requested, and the Socket 7 microprocessor gives up the bus on the next clock cycle. The module aborts the bus cycle that it is currently logging in (the Socket 7 microprocessor will restart this cycle once the BOFF# signal goes high). A backoff cycle will be logged in using one of the three interactions described for the HLDA signal (except that the BOFF# signal is stored as a low-level signal in each of the cases).

Mode Differences

The Socket 7 microprocessor can operate in either Component or Chip Set mode.

Component Mode

In Component mode (stand alone), the microprocessor interfaces directly to the system bus.

Chip Set Mode

The Socket 7 microprocessor, C5C cache controller, and the C8C cache memory (SRAM) can be combined to form a chip set or enhanced design. The two cache devices connect to the system bus and a memory bus controller interfaces to the microprocessor and cache devices.

The behavior of the Socket 7 microprocessor is affected when operating in Chip Set mode. The TMS 109A Socket 7 software and probe adapter still supports the Socket 7 microprocessor in this mode.

There are also two new signals: BRDYC# (pin L3) and ADSC# (pin N4).

In Component mode, the BRDYC# signal is seen as a “no connect” pin. The TMS 109A Socket 7 probe adapter uses the BRDYC# signal for clocking when it is active. The probe adapter has a pullup resistor on this line to hold it inactive when the Socket 7 is in Chip-Set mode. The BRDYC# signal can be probed on C1:0.

In Component mode, the ADSC# signal is seen as a “no connect” pin and is not used for clocking by the probe adapter.

Symbols

The TMS 109A Socket 7 support supplies one symbol table file. The SOCKET7_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file SOCKET7_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value D/P# INIT IRESET_L PRDY BUSCHK# SMIACT# LOCK# SCYC LAST_D AHOLD HLDA BOFF3# M/IO# D/C# W/R#	Meaning
RESET	X X 1 X X X X X X X X X X X X	Reset
P_FETCH	0 X 0 X X X 1 X X X 0 1 1 0 0	Primary processor opcode read
D_FETCH	1 X 0 X X X 1 X X X 0 1 1 0 0	Dual processor opcode read

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value D/P# PRDY SCYC BOFF3# INIT BUSCHK# LAST_D M/IO# IRESET_L SMIACT# AHOLD D/C# LOCK# HLDA W/R#	Meaning
FETCH*	X X 0 X X X 1 X X X 0 1 1 0 0	Opcode read
P_LOCK_RD	0 X 0 X X X 0 X X X 0 1 X 1 0	Primary processor locked read cycle
D_LOCK_RD	1 X 0 X X X 0 X X X 0 1 X 1 0	Dual processor locked read cycle
LOCK_RD*	X X 0 X X X 0 X X X 0 1 X 1 0	Locked read cycle
P_LOCK_WR	0 X 0 X X X 0 X X X 0 1 X 1 1	Primary processor locked write cycle
D_LOCK_WR	1 X 0 X X X 0 X X X 0 1 X 1 1	Dual processor locked write cycle
LOCK_WR*	X X 0 X X X 0 X X X 0 1 X 1 1	Locked write cycle
P_MEM_RD	0 X 0 X X X X X X X 0 1 1 1 0	Primary processor nonopcode read
D_MEM_RD	1 X 0 X X X X X X X 0 1 1 1 0	Dual processor nonopcode read
MEM_RD*	X X 0 X X X X X X X 0 1 1 1 0	Read from memory, nonopcode
P_MEM_WR	0 X 0 X X X X X X X 0 1 1 1 1	Primary processor write to memory
D_MEM_WR	1 X 0 X X X X X X X 0 1 1 1 1	Dual processor write to memory
MEM_WR*	X X 0 X X X X X X X 0 1 1 1 1	Write to memory
P_I/O_RD	0 X 0 X X X X X X X 0 1 0 1 0	Primary processor I/O read cycle
D_I/O_RD	1 X 0 X X X X X X X 0 1 0 1 0	Dual processor I/O read cycle
I/O_RD*	X X 0 X X X X X X X 0 1 0 1 0	I/O read cycle
P_I/O_WR	0 X 0 X X X X X X X 0 1 0 1 1	Primary processor I/O write cycle
D_I/O_WR	1 X 0 X X X X X X X 0 1 0 1 1	Dual processor I/O write cycle
I/O_WR*	X X 0 X X X X X X X 0 1 0 1 1	I/O write cycle
P_MEM_R/W*	0 X 0 X X X X X X X 0 1 1 1 X	Any primary processor read or write
D_MEM_R/W*	1 X 0 X X X X X X X 0 1 1 1 X	Any dual processor read or write
MEM_R/W*	X X 0 X X X X X X X 0 1 1 1 X	Any memory read or write cycle
P_I/O_R/W*	0 X 0 X X X X X X X 0 1 0 1 X	Any primary processor I/O cycle
D_I/O_R/W*	1 X 0 X X X X X X X 0 1 0 1 X	Any dual processor I/O cycle
I/O_R/W*	X X 0 X X X X X X X 0 1 0 1 X	Any I/O read or write cycle
P_READ*	0 X 0 X X X X X X X 0 1 X 1 0	Any primary processor read cycle
D_READ*	1 X 0 X X X X X X X 0 1 X 1 0	Any dual processor read cycle
READ*	X X 0 X X X X X X X 0 1 X 1 0	Any read cycle
P_WRITE*	0 X 0 X X X X X X X 0 1 X 1 1	Any primary processor write cycle
D_WRITE*	1 X 0 X X X X X X X 0 1 X 1 1	Any dual processor write cycle
WRITE*	X X 0 X X X X X X X 0 1 X 1 1	Any write cycle
P_INT_ACK	0 X 0 X X X X X X X 0 1 0 0 0	Primary processor int. acknowledge

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value D/P# PRDY SCYC BOFF3# INIT BUSCHK# LAST_D M/IO# IRESET_L SMIACT# AHOLD D/C# LOCK# HLDA W/R#	Meaning
D_INT_ACK	1 X 0 X X X X X X X 0 1 0 0 0	Dual processor int. acknowledge
INT_ACK*	X X 0 X X X X X X X 0 1 0 0 0	Interrupt acknowledge cycle
P_SPECIAL	0 X 0 X X X X X X X 0 1 0 0 1	Primary processor special cycle
D_SPECIAL	1 X 0 X X X X X X X 0 1 0 0 1	Dual processor special cycle
SPECIAL*	X X 0 X X X X X X X 0 1 0 0 1	Special cycle
P_RESERVE	0 X 0 X X X X X X X 0 1 1 0 1	Primary processor reserved
D_RESERVE	1 X 0 X X X X X X X 0 1 1 0 1	Dual processor reserved
RESERVE*	X X 0 X X X X X X X 0 1 1 0 1	Reserved
ALT_B_MTR	X X 0 X X X X X X X 1 X X X X	Alternate bus master cycle
BOFF	X X 0 X X X X X X X X 0 X X X	Backoff cycle
P_BUSCHCK	0 X 0 X 0 X X X X X 0 1 X X X	Primary processor buscheck
D_BUSCHCK	1 X 0 X 0 X X X X X 0 1 X X X	Dual processor buscheck
BUSCHCK*	0 X 0 X 0 X X X X X 0 1 X X X	Buscheck
P_LOCKED	0 X 0 X 1 X 0 X X X X X X X X	Any primary processor locked cycle
D_LOCKED	1 X 0 X 1 X 0 X X X X X X X X	Any dual processor locked cycle
LOCKED*	X X 0 X 1 X 0 X X X X X X X X	Any locked cycle
P_SPLTCYC*	0 X 0 X 1 X 0 1 X X X X X X X	Primary processor split cycle
D_SPLTCYC*	1 X 0 X 1 X 0 1 X X X X X X X	Dual processor split cycle
SPLTCYC*	X X 0 X 1 X 0 1 X X X X X X X	Split cycle
P_SMM*	0 X 0 X X 0 X X X X X X X X X	The primary processor is in smm
D_SMM*	1 X 0 X X 0 X X X X X X X X X	The dual processor is in smm
SMM*	X X 0 X X 0 X X X X X X X X X	Either processor is in smm
PRIMARY*	0 X X X X X X X X X X X X X X	Any primary processor cycle
DUAL*	1 X X X X X X X X X X X X X X	Any dual processor cycle

* **Symbols used only for triggering; they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquire data
- View disassembled data in various display formats
- Cycle type labels
- Change the way data is displayed
- Change disassembled cycles with the mark cycles function

NOTE. *The disassembly software is optimized to decode instruction streams and bus activities from Intel microprocessors and AMD-K6-2; therefore, the disassembler may not support unique characteristics of other manufacturers. However, you can reliably conduct timing analysis of nonIntel Socket 7 processors and use the high-level source debug capabilities of a Tektronix logic analyzer. Consult your Tektronix field office for future enhancements.*

Acquiring Data

Once you load the SOCKET7_ support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in five display formats: Timing, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–17.*

The default display format shows the Address, Data, Data_Lo, and Control channel groups for each sample of acquired data. The Data and Data_Lo groups are shown in one column.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
#	The pound sign is used to indicate an immediate value. This is somewhat dependent upon the target microprocessor assembler notation.
>	There is insufficient room on the screen to show all available data.
≫	The instruction was manually marked as a program fetch.
»	This instruction fetch cycle has been manually marked by the user (TLA 700).
t	This indicates the given number is in decimal. Example: #12t (for 0xC in hexadecimal)
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
*	A single asterisk at the beginning of the instruction implies the cycle is an out–of–order fetch. It is located in the first character to the left of the mnemonic.
c	A lower–case “c” is used to indicate a cache invalidation cycle. It is located in the second character to the left of the mnemonic.
–	A dash “–” is used to indicated that this cycle was issued by the “other” microprocessor, (Primary, or Dual, based on user selection).
(FLUSH)	The instruction has been flushed from the microprocessor’s internal instruction queue.
(16) or (32)	Indicates that the fetch is from a 16- or 32-bit code segment size, and disassembled accordingly. If the mnemonic fills the entire column width, the (16) or (32) will not be displayed.
SMM	Indicates a System management mode cycle.
(MMX)	Indicates an MMX instruction; appears at the end of the mnemonic.
(3DNow!)	Indicates an 3DNow! instruction; appears at the end of the mnemonic.

Table 2–2: Meaning of special characters in the display (cont.)

Character or string displayed	Meaning
??	This notation will be placed in a mnemonic field if the disassembler views the operand invalid for the instruction. For example, there is not a control register named “CR7”. Thus if the operand byte would indicate the register “CR7”, “(??)” will be placed to the right of the instruction string: “MOV CR7,EAX (??)”.
<more>	For Software Mode, if there are more than eight lines of text to be displayed for a cycle due to out-of-order fetching, the eighth line will have the text string “<more>” displayed at the right. This text WILL overlay any other text on the line (it has the highest priority).

Logic analyzer software does not allow more than 32 channels in each channel group. Therefore, two channel groups are used to acquire 64-bit wide Socket 7 microprocessor data.

To handle the display of disassembled data from both data groups, the disassembler may display more than one line for each data sample. For samples with two display lines, data displayed under the Data column of the first line is from the Data_Lo group (D31-0); data displayed under the Data column of the second line is from the Data group (D63-32). Figure 2–3 on page 2–14 shows examples of multiple display lines used to display Data_Lo and Data group information.

The disassembler synthesizes the A2-A0 signals.

Aborting Lengthy Disassembly. When acquiring data from two microprocessors, the disassembler might take a long time to display disassembled data. This could be caused by the combination of selections in the Trace Processor and Other Processor fields in the Disassembly property page (Disassembly Format Definition overlay).

An example where this might occur is when the Trace Processor field is set to DUAL, and the Other Processor field is set to Suppress. If the acquisition data only contains data from the Primary microprocessor, then the disassembler might take a long time to display disassembled cycle types or instruction mnemonics.

Timing-Waveform Display Format

In the Timing-Waveform display format, the display is set up to show the following waveforms:

CLK	D/C#	RESET
Address	M/IO#	HLDA
DataData_Lo	NA#	BOFF#
ADS#	CACHE#	AHOLD
D/P#	BRDY#	
W/R#	LOCK#	

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses (see Figure 2–9 on page 2–23). Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

The disassembler always displays at least one line of information. Because fetches should have valid data for the Data and Data_Lo groups, most fetches should use at least two display lines. For example, a fetch cycle can show both an instruction and a READ EXTENSION, or FLUSH (or both).

Table 2–3: Cycle type definitions

Label	Description
(RESET)	A reset cycle
(MEM READ)	A nonlocked memory read cycle that is not an opcode fetch
(LOCKED MEM READ)	A locked memory read cycle that is not an opcode fetch
(MEM WRITE)	Any nonlocked memory write
(LOCKED MEM WRITE)	Any locked memory write
(IO READ)	Read from an I/O port
(IO WRITE)	Write to an I/O port
(INT ACK)	Interrupt acknowledge cycle
(SHUTDOWN)	Shutdown/special bus cycle; BE7:BE0 = 11111110
(CACHE FLUSH)	Cache flush/special bus cycle; BE7:BE0 = 11111101
(HALT)	Halt/special bus cycle; BE7:BE0 = 11111011
(WRITE−BACK)	Write back/special bus cycle; BE7:BE0 = 11110111
(FLUSH ACK)	Flush Ack/special bus cycle; BE7:BE0 = 11101111
(BRANCH TRACE: TARGET)	Branch Trace Message/special bus cycle; BE7:BE0 = 11011111
(BRANCH TRACE: SOURCE)	Branch Trace Message/special bus cycle; BE7:BE0 = 11011111
(STOP GRANT ACK)	Stop Grant cycle; cycle type is HALT/SPECIAL; BE7:BE0 = 11111011

Table 2–3: Cycle type definitions (Cont.)

Label	Description
(RESERVED)	Reserved
(ALTERNATE BUS MASTER)	Bus is released to an Alternate Bus Master
(BACK OFF)	Back Off bus cycle
(UNKNOWN)	An invalid/unknown bus cycle
(BURST LINE FILL)*	Fetch cycle computed to be a burst fill. The data is fetched but will not be executed, it is part of a 32 byte fetch. It will possibly be stored in cache.
(BACKOFF/BURST FLUSH)*	Burst/Fetch cycle computed to be flushed due to a back off
(EXTENSION)*	Fetch cycle computed to be an opcode extension
(FLUSH)*	Fetch cycle computed to be flushed
(DUAL FETCH)	Nondisassembled fetch cycle from the Dual processor
(PRIMARY FETCH)	Nondisassembled fetch cycle from the Primary processor

* **Computed cycle types.**

Figure 2–3 shows an example of the Hardware display.

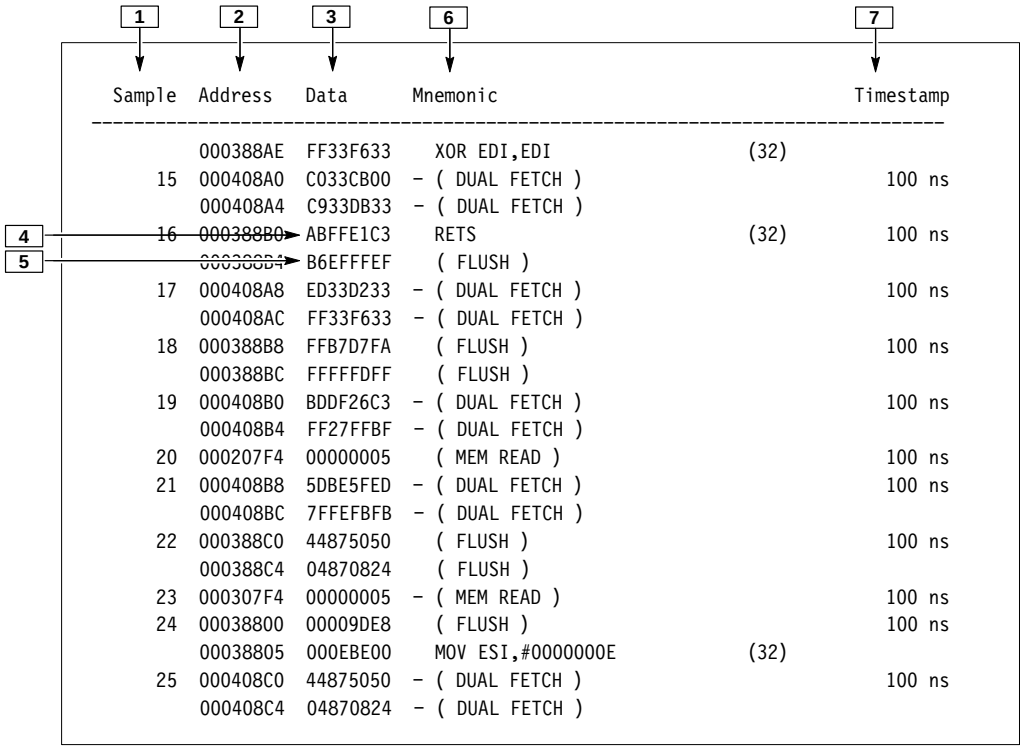


Figure 2–3: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the Socket 7 address bus.

3 **Data Column.** Lists data from channels connected to D63-D32 and/or D31-D0 of the Socket 7 microprocessor data bus. Refer to the general description of viewing disassembled data for information on how the disassembler determines when to display information for the Data group.

4 This part of the sample is displaying data from channels connected to D31-D0 of the Socket 7 microprocessor data bus.

5 This part of the sample is displaying data from channels connected to D63-D32 of the Socket 7 microprocessor data bus.

6 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

7 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed (see Figure 2–8 on page 2–22).

Out-of-order fetches are shown in the order the fetches are executed. An asterisk indicates an out-of-order fetch. The sample number of the out-of-order fetch will not be displayed if the previously executed instruction has a higher sample number. The sample number of the out-of-order fetch will be displayed if the previously executed instruction has a smaller sample number.

Since you cannot place the cursor on an instruction without a sample number, you will not be able to scroll to some out-of-order fetch instructions. To scroll to these instructions, you will have to switch to the Hardware display format. You also cannot mark an out-of-order fetch in software mode; you must switch to hardware mode.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the Socket 7 microprocessor are as follows:

CALL	IRET	RET
INT	JMP	RSM

Instructions that might generate a change in the flow of control in the Socket 7 microprocessor are as follows:

BOUND	JL/JNGE	JNP/JPO
DIV	JLE/JNG	JNS
IDIV	JNB/JAE/JNC	JO
INTO	JNBE/JA	JP/JPE
JB/JNAE/JC	JNE/JNZ	JS
JBE/JNA	JNL/JGE	LOOP
JCXZ/JECXZ	JNLE/JG	LOOPNZ/LOOPNE
JE/JZ	JNO	LOOPZ/LOOPE

If a conditional jump branches to an address that is reached sequentially (no address break in the fetch sample), the disassembler cannot determine if the branch was taken. If there are two conditional jump instructions close together that branch to the same fetch line, then the disassembler may not be able to determine which conditional jump was actually taken. You can use the mark cycle function to correct the disassembly. Refer to *Marking Cycles* later in this section.

MMX. Instructions that generate a trap in the flow of control in the Socket 7 microprocessor are as follows:

INT	IRET	RSM
CALL	RET	

Instructions that might generate a conditional trap in the flow of control in the Socket 7 microprocessor are as follows:

EMMS	MOVD	MOVQ	PACKSSD
PACKSSWB	PACKUSWB	PADDB	PADDD
PADDSB	PADDSW	PADDUSB	PADDUSW
PADDW	PAND	PANDN	PCMPEQB
PCMPEQD	PCMPEQW	PCMPGTB	PCMPGTD
PCMPGTW	PMADDWD	PMULHW	PMULLW
POR	PSLLD	PSLLQ	PSLLW
PSRAD	PSRAW	PSRLD	PSRLQ
PSRLW	PSUBB	PSUBD	PSUBSB
PSUBSW	PSUBUSB	PSUBUSW	PSUBW
PUNPCKHBW	PUNPCKHDQ	PUNPCKHWD	PUNPCKLBW
PUNPCKLDQ	PUNPCKLWD	PXOR	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the Socket 7 microprocessor are as follows:

CALL	INT	IRET
RET	RSM	

Instructions that might generate a subroutine call or a return in the Socket 7 microprocessor are as follows:

BOUND	DIV	IDIV	INTO

MMX. Instructions that generate a trap in the flow of control in the Socket 7 microprocessor are as follows:

INT	IRET	RSM
CALL	RET	

Instructions that might generate a conditional trap in the flow of control in the Socket 7 microprocessor are as follows:

EMMS	MOVD	MOVQ	PACKSSDW
PACKSSWB	PACKUSWB	PADDB	PADDD
PADDSB	PADDSW	PADDUSB	PADDUSW

PADDW	PAND	PANDN	PCMPEQB
PCMPEQD	PCMPEQW	PCMPGTB	PCMPGTD
PCMPGTW	PMADDWD	PMULHW	PMULLW
POR	PSLLD	PSLLQ	PSLLW
PSRAD	PSRAW	PSRLD	PSRLQ
PSRLW	PSUBB	PSUBD	PSUBSB
PSUBSW	PSUBUSB	PSUBUSW	PSUBW
PUNPCKHBW	PUNPCKHDQ	PUNPCKHWD	PUNPCKLBW
PUNPCKLDQ	PUNPCKLWD	PXOR	

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the Socket 7 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

***NOTE**. All information defined in these fields pertain to the microprocessor that is being traced.*

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the code segment size
- Choose an interrupt table
- Specify the starting address of the interrupt table
- Specify the size of the interrupt table
- Select to trace the Primary or Dual microprocessor
- Choose whether to display or suppress the hardware cycles from the microprocessor not being traced

The Socket 7 support has six additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, Interrupt Table Size, Trace Processor, and Other Processor. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32-bit or 16-bit. The default code size is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Trace Processor. You can select to disassemble data from the Primary or Dual microprocessor. The default is Primary.

Processor. You can specify either Intel or AMD depending on the socket7 processor that is under test. The TMS 109A Socket 7 support has been tested with both these microprocessor venders.

Other Processor. The “other” microprocessor is the one not being traced (not selected in the Trace Processor field). You can select to display or to suppress its bus cycles.

Dual Microprocessors Execution Tracing

When acquiring data from a system under test with two microprocessors, the disassembler can trace the execution flow of one microprocessor and display the hardware cycle types of the microprocessor not being traced. This means that the software disassembles only the instructions executed from the microprocessor being traced.

You can trace instructions from either the Primary microprocessor or the Dual microprocessor. You can also choose to display or not display (suppress) data from the microprocessor not selected in the Trace Processor field of the Disassembly property page (Disassembly Format Definition overlay).

To set up the mode of tracing, you need to set the Trace Processor and Other Processor fields in the Disassembly property page. Table 2–4 shows the combinations of Trace Processor and Other Processor field selections and their effects.

Table 2–4: Trace Processor and Other Processor field selections

Trace processor	Other processor	Effect
Primary	Suppress	Disassemble the Primary microprocessor only
Primary	Display Cycles	Disassemble the Primary microprocessor and display the hardware cycles of the Dual microprocessor
Dual	Suppress	Disassemble the Dual microprocessor only
Dual	Display Cycles	Disassemble the Dual microprocessor and display the hardware cycles of the Primary microprocessor

Figure 2–4 shows disassembled data from the Primary microprocessor and hardware cycles from the other microprocessor. A hyphen to the left of the mnemonic indicates data from the other microprocessor.

```
  Sample  Address   Data      Mnemonic                              Control
-------------------------------------------------------------------------------
      16  000388B0  ABFFE1C3    RETS                        (32)  P_FETCH
          000388B4  B6EFFFEF    ( FLUSH )                       P_FETCH
      17  000408A8  ED33D233  - ( DUAL FETCH )                   D_FETCH
          000408AC  FF33F633  - ( DUAL FETCH )                   D_FETCH
      18  000388B8  FFB7D7FA    ( FLUSH )                       P_FETCH
          000388BC  FFFFFDFF    ( FLUSH )                       P_FETCH
      19  000408B0  BDDF26C3  - ( DUAL FETCH )                   D_FETCH
          000408B4  FF27FFBF  - ( DUAL FETCH )                   D_FETCH
      20  000207F4  00000005    ( MEM READ )                    P_MEM_RD
      21  000408B8  5DBE5FED  - ( DUAL FETCH )                   D_FETCH
          000408BC  7FFEFBFB  - ( DUAL FETCH )                   D_FETCH
      22  000388C0  44875050    ( FLUSH )                       P_FETCH
          000388C4  04870824    ( FLUSH )                       P_FETCH
      23  000307F4  00000005  - ( MEM READ )                    D_MEM_RD
      24  00038800  00009DE8    ( FLUSH )                       P_FETCH
          00038805  000EBE00    MOV ESI,#0000000E           (32)  P_FETCH
      25  000408C0  44875050  - ( DUAL FETCH )                   D_FETCH
          000408C4  04870824  - ( DUAL FETCH )                   D_FETCH
      26  0003880A  0AB90000    MOV ECX,#0000000A           (32)  P_FETCH
          0003880F  F3000000    REPZ                        (32)  P_FETCH
```

Figure 2–4: Data displayed from the Primary and Dual microprocessors

Figure 2–5 shows disassembled data from the Primary microprocessor only. Data from the Dual microprocessor is suppressed and not displayed.

Sample	Address	Data	Mnemonic		Control
16	000388B0	ABFFE1C3	RETS	(32)	P_FETCH
	000388B4	B6EFFFEF	(FLUSH)		P_FETCH
18	000388B8	FFB7D7FA	(FLUSH)		P_FETCH
	000388BC	FFFFFDFF	(FLUSH)		P_FETCH
20	000207F4	00000005	(MEM READ)		P_MEM_RD
22	000388C0	44875050	(FLUSH)		P_FETCH
	000388C4	04870824	(FLUSH)		P_FETCH
24	00038800	00009DE8	(FLUSH)		P_FETCH
	00038805	000EBE00	MOV ESI,#0000000E	(32)	P_FETCH
26	0003880A	0AB90000	MOV ECX,#0000000A	(32)	P_FETCH
	0003880F	F3000000	REPZ	(32)	P_FETCH
28	00038810	003668AD	LODSD	(32)	P_FETCH
	00038811	003668AD	PUSH #00000036	(32)	P_FETCH
	00038816	026A0000	PUSH #02	(32)	P_FETCH
30	00038818	4668026A	PUSH #02	(32)	P_FETCH
	0003881A	4668026A	PUSH #00000046	(32)	P_FETCH
	0003881F	6A000000	PUSH #02	(32)	P_FETCH

Figure 2–5: Disassembled data displayed from the Primary microprocessor only

Figure 2–6 shows disassembled data from the Dual microprocessor only. Data from the Primary microprocessor is suppressed and not displayed.

Sample	Address	Data	Mnemonic		Control
17	000408A8	ED33D233	XOR EDX,EDX	(32)	D_FETCH
	000408AA	ED33D233	XOR EBP,EBP	(32)	D_FETCH
	000408AC	FF33F633	XOR ESI,ESI	(32)	D_FETCH
	000408AE	FF33F633	XOR EDI,EDI	(32)	D_FETCH
19	000408B0	BDDF26C3	RETS	(32)	D_FETCH
	000408B4	FF27FFBF	(FLUSH)		D_FETCH
21	000408B8	5DBE5FED	(FLUSH)		D_FETCH
	000408BC	7FFEFBFB	(FLUSH)		D_FETCH
23	000307F4	00000005	(MEM READ)		D_MEM_RD
25	000408C0	44875050	(FLUSH)		D_FETCH
	000408C4	04870824	(FLUSH)		D_FETCH
27	00040800	00009DE8	(FLUSH)		D_FETCH
	00040805	000EBE00	MOV ESI,#0000000E	(32)	D_FETCH
29	0004080A	0AB90000	MOV ECX,#0000000A	(32)	D_FETCH
	0004080F	F3000000	REPZ	(32)	D_FETCH

Figure 2–6: Disassembled data displayed from the Dual microprocessor only

Branch Trace Messages

The disassembler interprets the information on the Address and Data Bus of Branch Trace Messages (BTMs) by reconstructing the address of the source or target of the branch instruction. Depending on which type of BTM is in use, either fast or normal, one or two BTMs will appear on the bus. The disassembler tracks BTMs as they appear on the bus. Figure 2–7 shows how the disassembler displays these cycles.

Sample	Address	Data	Mnemonic	Control
4	000207F4	00000005	(MEM WRITE)	P_MEM_WR
6	00038810	003868AD	(FLUSH)	P_FETCH
	00038814	026A0000	(FLUSH)	P_FETCH
8	000388A2	20------	(BRANCH TRACE: TARGET)	P_SPECIAL
10	00038800	08------	(BRANCH TRACE: SOURCE)	P_SPECIAL
14	00038818	33C03300	(FLUSH)	P_FETCH
	00038810	68C933DB	(FLUSH)	P_FETCH

Figure 2–7: Display of target and source Branch Trace Messages

Out-Of-Order Fetches

The Socket 7 microprocessor can prefetch cycles out of ascending order. For example, a branch to address 1008 could cause the following sample of addresses across the bus: 1008, 1000, 1018, and 1010. The data at address 1008 is executed, but the data at address 1000 is not. The data at addresses 1018 and 1010 are executed, but the data at address 1010 is executed before the data at 1018.

An example of the Intel fetched order versus the executed order is shown below.

Fetched Order	Executed Order
1008	1008
1000	1010
1018	1018
1010	

The AMD socket has an out-of-order bus. An example of the AMD fetched order versus the executed order is shown below.

Fetched Order	Executed Order
1018	1000
1010	1008
1008	1010
1000	1018

In the Hardware display format, the out-of-order fetches are displayed in the order they are fetched. They will be properly disassembled and identified by an asterisk (*) to the left of the instruction (see Figure 2–9 on page 2–23).

In the Hardware display format, you can determine the executed order of the out-of-order fetches by looking at the address of the out-of-order cycles and the subsequent cycles. Fetch cycles always have the sample numbers displayed.

In the Software display format, out-of-order fetches are displayed in the order they were executed (see Figure 2–8). If the previously executed instruction had a larger sample number than the out-of-order fetch, the sample number will not be displayed. If the previous sample number is smaller than the out-of-order fetch, the sample number will be displayed. To mark an instruction without a sample number, switch to the Hardware display format (see Figure 2–9 on page 2–23).

Sample	SOCKET7 Address	SOCKET7 Data	Address	SOCKET7 Mnemonic	SOCKET7 Control	Cache	Timestamp
	0002000C	F633ED33		*XOR EBP,EBP (32)	P_FETCH		
	0002000E	F633ED33		*XOR ESI,ESI (32)	P_FETCH		
	00020010	9BC3FF33		*XOR EDI,EDI (32)	P_FETCH		
	00020012	9BC3FF33		*RETS (32)	P_FETCH		
252	0001F7F0	0FD8F20F	0001F7F0	*PSLLD MM3,MM0 (MMX) (32)	P_FETCH	1	23.634,500 us
	0001F7F3	0FD8F20F		*PSLLD MM3,#CC (MMX) (32)	P_FETCH		
	0001F7F7	0FCCF372		*PSLLQ MM2,MM1 (MMX) (32)	P_FETCH		
	0001F7FA	48E9D1F3		*JMPS 0001F847 (32)	P_FETCH		
258	0001F847	0FFFFFFE	0001F840	PSUBSW MM3,[EBX] (MMX) (32)	P_FETCH	1	24.373,000 us
	0001F84A	589C1BE9		*PUSHFD (32)	P_FETCH		
	0001F84B	589C1BE9		*POP EAX (32)	P_FETCH		
	0001F84C	FFFFBE25		*AND EAX,#FFFFFFBE (32)	P_FETCH		
	0001F851	0F9D50FF		*PUSH EAX (32)	P_FETCH		
	0001F852	0F9D50FF		*POPFD (32)	P_FETCH		
	0001F853	0F9D50FF		*JNBE 0001F86F (32)	P_FETCH		
270	0001F86F	0F909000	0001F868	*PMULHRW MM7,MM1 (3DNow!) (32)	P_FETCH	1	26.169,000 us
	0001F873	0FB7F90F		*PAVGUSB MM1,[EAX] (3DNow!) (32)	P_FETCH		
	0001F877	9CBF080F		*PUSHFD (32)	P_FETCH		
	0001F878	00010D58		*POP EAX (32)	P_FETCH		
	0001F879	00010D58		*OR EAX,#00000001 (32)	P_FETCH		
	0001F87E	9D500000		*PUSH EAX (32)	P_FETCH		
	0001F87F	9D500000		*POPFD (32)	P_FETCH		
279	0001F880	9090D872	0001F880	JB 0001F85A (32)	P_FETCH	1	27.555,500 us
286	0001F85A	0F0F9000	0001F858	*PFCMPEQ MM2,[EDX] (3DNow!) (32)	P_FETCH	1	28.513,500 us
	0001F85E	589CB012		*PUSHFD (32)	P_FETCH		
	0001F85F	589CB012		*POP EAX (32)	P_FETCH		
296	0001F860	FFFFFE25	0001F860	AND EAX,#FFFFFFFE (32)	P_FETCH	1	29.870,000 us
	0001F865	0F9D50FF		PUSH EAX (32)	P_FETCH		
	0001F866	0F9D50FF		POPFD (32)	P_FETCH		
	0001F867	0F9D50FF		JNB 0001F8C1 (32)	P_FETCH		
306	0001F8C1	380F0FA6	0001F8C0	PMULHRW MM7,[EAX] (3DNow!) (32)	P_FETCH	1	31.197,000 us
	0001F8C5	590F0FB7		PAVGUSB MM3,08[ECX] (3DNow!) (32)	P_FETCH		
	0001F8CA	0F0FBF08		*PF2ID MM5,08[EBP] (3DNow!) (32)	P_FETCH		
	0001F8CF	9C1D086D		*PUSHFD (32)	P_FETCH		
	0001F8D0	00410D58		*POP EAX (32)	P_FETCH		
	0001F8D1	00410D58		*OR EAX,#00000041 (32)	P_FETCH		
	0001F8D6	9D500000		*PUSH EAX (32)	P_FETCH		
	0001F8D7	9D500000		*POPFD (32)	P_FETCH		
	0001F8D8	000486OF		*JBE 0001F8E2 (32)	P_FETCH		
322	0001F8E2	589C9090	0001F8E0	PUSHFD (32)	P_FETCH	1	33.901,000 us
	0001F8E3	589C9090		POP EAX (32)	P_FETCH		
	0001F8E4	0000010D		OR EAX,#00000001 (32)	P_FETCH		
	0001F8E9	0F9D5000		*PUSH EAX (32)	P_FETCH		
	0001F8EA	0F9D5000		*POPFD (32)	P_FETCH		
	0001F8EB	0F9D5000		*JB 0001F8FE (32)	P_FETCH		
331	0001F8FE	0F9C90B6	0001F8F8	*PUSHFD (32)	P_FETCH	1	35.148,000 us
	0001F8FF	0F9C90B6		*PAVGUSB MM7,[EDX] (3DNow!) (32)	P_FETCH		
339	0001F903	0FBF3A0F	0001F900	PF2ID MM0,[EAX] (3DNow!) (32)	P_FETCH	1	36.145,500 us
	0001F907	0F1D000F		PFACC MM6,[EDI] (3DNow!) (32)	P_FETCH		
	0001F90B	58AE370F		*POP EAX (32)	P_FETCH		
	0001F90C	0000010D		*OR EAX,#00000001 (32)	P_FETCH		
	0001F911	0F9D5000		*PUSH EAX (32)	P_FETCH		
	0001F912	0F9D5000		*POPFD (32)	P_FETCH		
	0001F913	0F9D5000		*JNB 0001FB5D (32)	P_FETCH		

Figure 2–8: Software display for the AMD Bus cycles

Sample	SOCKET7 Address	SOCKET7 Data	Address	SOCKET7 Mnemonic	SOCKET7 Control	Cache	Timestamp
280	0001F71C	00000207	0001F71C	(MEM WRITE)	P_MEM_WR	1	27.595,500 us
281	0001F71C	00000207	0001F71C	(MEM READ)	P_MEM_RD	1	27.845,000 us
282	0001F8B8	9408520F	0001F8B8	*(FLUSH)	P_FETCH	1	28.074,500 us
	0001F8BC	08650F0F		*(FLUSH)	P_FETCH		
283	0001F8B0	0F0FB73F	0001F8B0	*(FLUSH)	P_FETCH	1	28.184,000 us
	0001F8B4	0FAE084D		*(FLUSH)	P_FETCH		
284	0001F8A8	0F000002	0001F8A8	*(FLUSH)	P_FETCH	1	28.294,000 us
	0001F8AC	0F0F3668		*(FLUSH)	P_FETCH		
285	0001F8A0	0F000002	0001F8A0	(FLUSH)	P_FETCH	1	28.403,500 us
	0001F8A4	8E128CD9		(FLUSH)	P_FETCH		
286	0001F85A	0F0F9000	0001F858	*PFCMPEQ MM2,[EDX] (3DNow!) (32)	P_FETCH	1	28.513,500 us
	0001F85E	589CB012		*PUSHFD (32)	P_FETCH		
	0001F85F	589CB012		*POP EAX (32)	P_FETCH		
287	0001F850	0F9D50FF	0001F850	*(FLUSH)	P_FETCH	1	28.623,000 us
	0001F854	00001687		*(FLUSH)	P_FETCH		
288	0001D000	00000000	0001D000	(MEM READ)	P_MEM_RD	1	28.802,500 us
	0001D004	00000000		(MEM READ)	P_MEM_RD		
289	0001F848	589C1BE9	0001F848	*(FLUSH)	P_FETCH	1	28.982,500 us
	0001F84C	FFFFBE25		*(FLUSH)	P_FETCH		
290	0001F71C	00000207	0001F71C	(MEM WRITE)	P_MEM_WR	1	29.022,000 us
291	0001F840	F6E900F9	0001F840	(FLUSH)	P_FETCH	1	29.122,000 us
	0001F844	0FFFFFFE		(FLUSH)	P_FETCH		
292	0001F71C	00000207	0001F71C	(MEM READ)	P_MEM_RD	1	29.361,500 us
293	0001F878	00010D58	0001F878	*(FLUSH)	P_FETCH	1	29.541,000 us
	0001F87C	9D500000		*(FLUSH)	P_FETCH		
294	0001F870	0FB7F90F	0001F870	*(FLUSH)	P_FETCH	1	29.650,500 us
	0001F874	9CBF080F		*(FLUSH)	P_FETCH		
295	0001F868	00005483	0001F868	*(EXTENSION)	P_FETCH	1	29.760,500 us
	0001F86C	0F9D9000		*(EXTENSION)	P_FETCH		
296	0001F860	FFFFFE25	0001F860	AND EAX,#FFFFFFFE (32)	P_FETCH	1	29.870,000 us
	0001F865	0F9D50FF		PUSH EAX (32)	P_FETCH		
	0001F866	0F9D50FF		POPFD (32)	P_FETCH		
	0001F867	0F9D50FF		JNB 0001F8C1 (32)	P_FETCH		
297	0001F71C	00000206	0001F71C	(MEM WRITE)	P_MEM_WR	1	29.940,000 us
298	0001F71C	00000206	0001F71C	(MEM READ)	P_MEM_RD	1	30.189,500 us
299	0001F898	0FCAE10F	0001F898	*(FLUSH)	P_FETCH	1	30.429,000 us
	0001F89C	8E3D24D8		*(FLUSH)	P_FETCH		
300	0001F890	0000028E	0001F890	*(FLUSH)	P_FETCH	1	30.538,500 us
	0001F894	CCF4730F		*(FLUSH)	P_FETCH		
301	0001F888	3F0F0FB0	0001F888	*(FLUSH)	P_FETCH	1	30.648,500 us
	0001F88C	8BE50FA6		*(FLUSH)	P_FETCH		
302	0001F880	9090D872	0001F880	(FLUSH)	P_FETCH	1	30.758,000 us
	0001F884	1A0F0F90		(FLUSH)	P_FETCH		
303	0001F8D8	0004860F	0001F8D8	*JBE 0001F8E2 (32)	P_FETCH	1	30.868,000 us
	0001F8DC	90900000		*(EXTENSION)	P_FETCH		
304	0001F8D0	00410D58	0001F8D0	*POP EAX (32)	P_FETCH	1	30.977,500 us
	0001F8D1	00410D58		*OR EAX,#00000041 (32)	P_FETCH		
	0001F8D6	9D500000		*PUSH EAX (32)	P_FETCH		
	0001F8D7	9D500000		*POPFD (32)	P_FETCH		
305	0001F8CA	0F0FBF08	0001F8C8	*PF2ID MM5,08[EBP] (3DNow!) (32)	P_FETCH	1	31.087,500 us
	0001F8CF	9C1D086D		*PUSHFD (32)	P_FETCH		
306	0001F8C1	380F0FA6	0001F8C0	PMULHRW MM7,[EAX] (3DNow!) (32)	P_FETCH	1	31.197,000 us
	0001F8C5	590F0FB7		PAVGUSB MM3,08[ECX] (3DNow!) (32)	P_FETCH		
307	0001F8F8	3B0F0FB6	0001F8F8	*(FLUSH)	P_FETCH	1	31.516,500 us

Figure 2–9: Hardware display for the AMD Bus cycles

Speculative Prefetch Cycles

Speculative prefetch cycles can occur when the Socket 7 microprocessor fetches instructions that have been previously executed. To minimize prefetch delays, the Socket 7 microprocessor predicts the outcome of the branch instruction and starts prefetching at that address. When the branch instruction is executed, the target address is determined. If the Socket 7 microprocessor predicted the target address correctly, then the needed code has already been fetched. If it did not correctly predict the target address, then the speculative prefetch cycles that had been fetched will be flushed and fetching will begin at the target address.

Figure 2–10 shows an example of speculative prefetch cycles. The previous time (not shown) that the JNE instruction was executed, the branch was taken and the new target address was 0x3893D. The microprocessor assumed that the address would be 0x3893D and so started fetching at 0x38938 (which contains 0x3893D). Cycles at samples 746 and 748 are speculative prefetch cycles. When the instruction was executed, the microprocessor determined that the branch was

not taken, flushed the speculative prefetch cycles, and started fetching at 0x38988 (sample 750), which contained the next instruction after the JNE.

Sample	Address	Data	Mnemonic		Control
	00038986	B575C90F	JNE 0003893D	(32)	P_FETCH
734	000207D8	00000008	(MEM READ)		P_MEM_RD
736	000207E8	00000046	(MEM READ)		P_MEM_RD
738	00038988	000000BA	(FLUSH)		P_FETCH
	0003898C	24558900	(FLUSH)		P_FETCH
740	00038990	20C2619D	(FLUSH)		P_FETCH
	00038994	6FBF6D00	(FLUSH)		P_FETCH
742	00038998	CDBFDE6F	(FLUSH)		P_FETCH
	0003899C	FFEFFFF7	(FLUSH)		P_FETCH
744	000389A0	FFFFEDAE	(FLUSH)		P_FETCH
	000389A4	F6FFF7EF	(FLUSH)		P_FETCH
746	00038938	DB9BFF33	(FLUSH)		P_FETCH
	0003893C	0002A3E3	(FLUSH)		P_FETCH
748	00038940	6D8A0000	(FLUSH)		P_FETCH
	00038944	204D8A10	(FLUSH)		P_FETCH
750	00038988	000000BA	MOV EDX,#00000000	(32)	P_FETCH
	0003898D	24558900	MOV 24[EBP],EDX	(32)	P_FETCH

Figure 2–10: Speculative Prefetch cycles

NOTE. *The microprocessor also has a Branch Target Buffer and often performs speculative prefetching of branch target addresses (no matter if they are taken or are not taken). The disassembler usually interprets the correct flow of execution but cannot do so deterministically.*

Cache Invalidation Cycles

Cache Invalidation cycles are needed to keep the microprocessor cache contents consistent with external memory. On a nonburst cycle that is also a Cache Invalidation cycle, the data and address will be valid as probed. On a burst cycle that is also a Cache Invalidation cycle, the data will be valid, but the addresses will not be valid as probed and the software will try to calculate the address from the surrounding cycles. Fetch cycles are disassembled. A letter `c` to the left of the mnemonic indicates a Cache Invalidation cycle, where the AHOLD signal was active.

Burst Cycles

On all burst cycles, only the first cycle contains a valid address. The Socket 7 microprocessor does not increment the address for a burst. The disassembler calculates the remaining burst cycle addresses for display.

System Management Mode (SMM)

The Socket 7 microprocessor provides a special mode called System Management Mode where the Socket 7 microprocessor CPU executes code from a

separate, alternate memory space called SMRAM. The disassembler uses information from the SMIACT# signal to determine when the Socket 7 microprocessor is operating in this mode.

MMX Instruction Set

The Socket 7 microprocessor includes the MMX instruction set. Since these instructions are potential subroutine instructions, the disassembler checks to see if an interrupt level 6 (illegal opcode) or 7 (device not available) occurred. If an interrupt 6 or 7 occurs, the interrupt will flush the bus.

When the disassembler detects that an instruction is from the MMX set, it displays an (MMX) to the right of the mnemonic.

MMX instructions are disassembled whether or not the microprocessor is set up to execute them.

3DNow!

The Socket 7 microprocessor includes the 3DNow! instruction set which supports AMD-K6-2. When the disassembly detects that an instruction is from the 3DNow! set, it displays (3DNow!) to the right of the mnemonics.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode & Flush Previous (marks the first word of an instruction and the lower bytes of this cycle as flushed)
- Opcode (marks the first word of an instruction)
- Flush to end (flushes the current byte to the high end of the sample)
- Flush (marks an opcode or extension that is fetched but not executed)
- Undo (clears all marks on this byte)
- Flush Cycle (the entire cycle was fetched, but not executed (opcode or extension))
- 16-bit or 32-bit default segment size

Mark selections are as follows:

```
Lo: --   --   --   00
Lo: --   --   11   --
Lo: --   22   --   --
Lo: 33   --   --   --
Hi: --   --   --   44
Hi: --   --   55   --
Hi: --   66   --   --
```

```
Hi: 77    --    --    --
FLUSH CYCLE
16-bit Default Segment Size
32-bit Default Segment Size
Undo marks on this cycle
```

You can use the Mark Opcode function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of the cycle is independent of any prefix override bytes in the particular fetch. For example, if you mark cycle 455 with a default size of 32 bits, but there are address/operand override prefixes in the instruction, the default size will be 32 bits but the size of the instruction will be 16 bits.

Only one selection can be made at a time. If the you want to mark both the opcode and default size of a particular cycle, it must be done in two different steps.

When marking opcodes of out-of-order fetches, and displaying in Software mode, and an out-of-order fetch does not have a sequence number, you must switch to hardware mode to mark that sequence. See *Out-Of-Order Fetches* on page 2–21 and *Software Display Format* on page 2–15.

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected modes in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–5 lists the Socket 7 exception vectors for the Real Addressing mode.

Table 2–5: Exception vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT

Table 2–5: Exception vectors for Real Addressing mode (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	DEVICE NOT AVAILABLE
8	0020	DOUBLE DEFAULT
9	0024	RESERVED
10	0028	RESERVED
11	002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR ERROR
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

***** **IV means interrupt vector.**

Table 2–6 lists the Socket 7 exception vectors for the Protected Addressing mode.

Table 2–6: Exception vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT

Table 2–6: Exception vectors for Protected Addressing mode (cont.)

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
12	0060	STACK EXCEPTION
13	0068	SEGMENT OVERRUN
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17	0088	ALIGNMENT CHECK
18	0090	MACHINE CHECK
19-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

*** IDT means interrupt descriptor table.**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your Socket 7 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and two sockets for a Socket 7 microprocessor. The probe adapter connects to the microprocessor in the system under test. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the supplied power adapter.

The probe adapter accommodates the Intel Pentium, low-power embedded Pentium with MMX technology, and Socket 7 microprocessors devices.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a system under test. Table 3–1 shows the electrical requirements the system under test must produce for the support to acquire correct data.

In Table 3–1 one podlet load is 20 kΩ in parallel with 2 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
System under test DC power requirements		
Voltage	4.75 – 5.25 VDC	
Current	I maximum (calculated) 1.8 A I typical (measured)1.2 A	
Probe adapter power supply requirements		
Voltage	90 – 265 VAC	
Current	1.1 A maximum at 100 VAC	
Frequency	47 – 63 Hz	
Power	25 W maximum	
System under test clock		
Clock rate Tested cock rate	Maximum 100 MHz Maximum 100 MHz	
Minimum setup time required	3.0 ns	
Minimum hold time required	0 ns	
	AC load	**DC load**
Measured typical SUT signal loading		
CLK	25 pF	1 CDC2510B|| (500ohms+30pF)
ADS#, ADSC#, W/R#, BRDY#, HLDA, BE7–0#, BOFF#	5 pF	1 22LV10
RESET	5 pF	1 22LV10
All other signals	2 pF	1 22LV10

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed Socket 7 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Figure 3–1 shows the dimensions of the probe adapter.

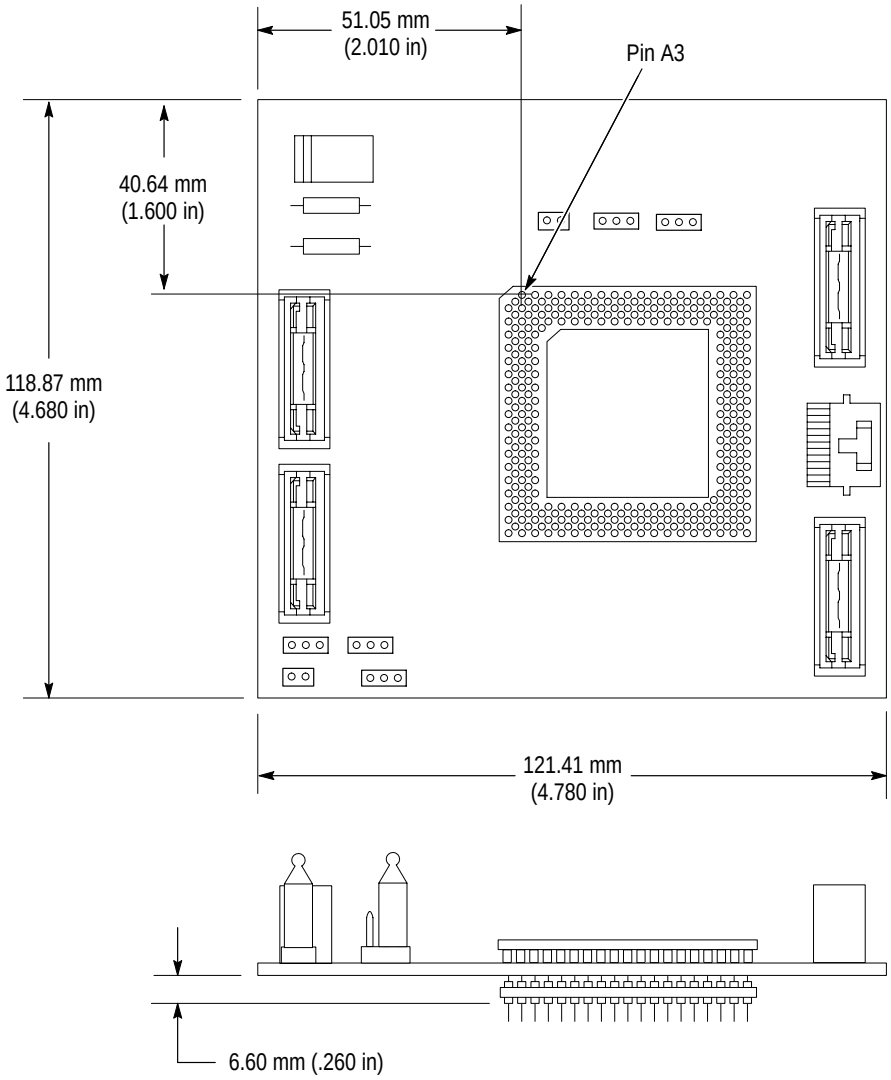


Figure 3–1: Dimensions of the probe adapter

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The active components on the probe adapter are: five GAL 22V10D PALs for signal synthesis, one LM3940ISX for 5 V to 3.3 V conversion, and one PPL-Buffer and one PLL (phase locked loop) low-skew clock generator for clock distribution with buffer.

The PALs implement three sequential state machines that monitor the Socket 7 microprocessor bus and generate three important signals:

- PIPED_D indicates Socket 7 microprocessor bus pipelining is occurring
- LAST_D indicates the end of a Socket 7 microprocessor bus cycle
- DVALID_D indicates valid data is present on the Socket 7 microprocessor data bus

These signals are required for the Clocking State Machine (CSM) of the logic analyzer to accurately strobe addresses and data information from the Socket 7 microprocessor bus.

The CSM is tightly linked to the processor bus T-states and is synchronized to the Socket 7 microprocessor on a clock by clock basis. It is possible that unpredictable bus behavior by an alternate bus master may cause the bus tracking machines to lose track of the bus. If this occurs, the bus tracking mechanism will automatically re-synchronize and reset itself when the Socket 7 microprocessor exits bus back off or bus hold.

If resynchronizing and reseting the bus tracking machines is not adequate, jumper J920 will disable the bus tracking PALs during any alternate bus master (HLDA) cycle or back off (BOFF #) cycle. If you disable the bus tracking PALs, acquisition of back off or hold cycles are inhibited, and one sample containing unusable information is recorded to show a cycle occurred.

A 20-pin connector, Intel In-Target Probe (ITP), is located on the probe adapter. Your system under test has system reset circuitry that can not be accessed through the SPGA socket, but you may connect the DBRESET signal (or the active low, open collector version OC_DBRESET*) to your system reset circuitry externally.

A PLL clock generator is used to provide eight, zero-delay copies of the Socket 7 microprocessor CLK input that are distributed to the PALs. Lock time after VCC is a 500 μS maximum, the clock is stable before any Socket 7 microprocessor bus cycles start. Table 4–1 lists Socket 7 signal delays when using the probe adapter.

Table 4–1: Socket 7 signal delays using the probe adapter

Signal name	Hardware CLK delays	Firmware CLK delays
A31:3, D63:0, BE7-0#, D/C#, M/IO#, PRDY, LOCK#, BUSCHK#, SMIACT#, INIT, SCYC, D/P#, AHOLD	0	2
HLDA, ADS#, BRDY#	2	0
BOFF#	2	1
RESET, NA#	1	0
W/R#	2	1

Replacing the Fuse

If the fuse on the Socket 7 probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter board.

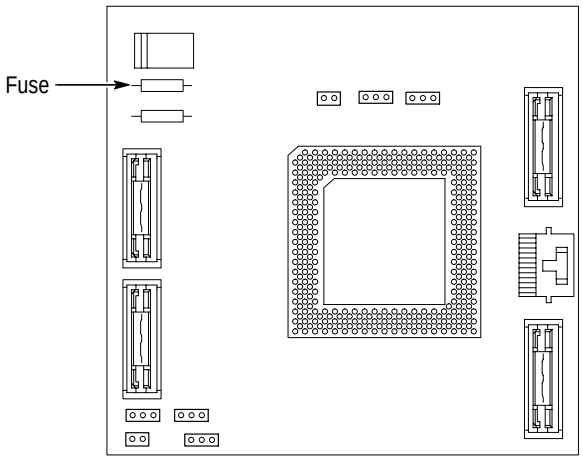


Figure 4–1: Location of the fuse on the probe adapter

Diagrams

Diagrams and Circuit Board Illustrations

This section contains the troubleshooting procedures, block diagrams, circuit board illustrations, component locator tables, waveform illustrations, and schematic diagrams.

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975. Abbreviations are based on ANSI Y1.1-1972.

Logic symbology is based on ANSI/IEEE Standard 91-1984 in terms of positive logic. Logic symbols depict the logic function performed and can differ from the manufacturer's data.

The Tilde (~) after a signal name indicates that the signal performs its intended function when in the low state.

Other standards used in the preparation of diagrams by Tektronix, Inc., include the following:

- Tektronix Standard 062-2476 Symbols and Practices for Schematic Drafting
- ANSI Y14.159-1971 Interconnection Diagrams
- ANSI Y32.16-1975 Reference Designations for Electronic Equipment
- MIL-HDBK-63038-1A Military Standard Technical Manual Writing Handbook

Component Values

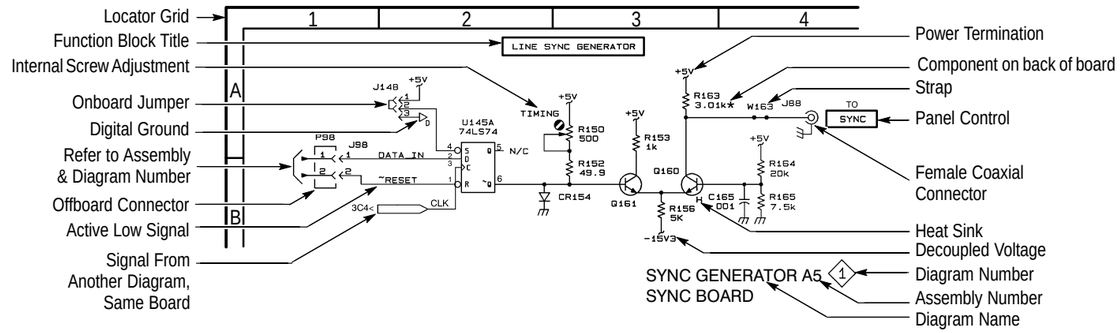
Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors: Values one or greater are in picofarads (pF).
Values less than one are in microfarads (F).

Resistors: Values are in Ohms (Ω).

Graphic Items and Special Symbols Used in This Manual

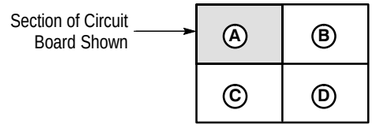
Each assembly in the instrument is assigned an assembly number (for example A5). The assembly number appears in the title on the diagram, in the lookup table for the schematic diagram, and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assembly in numerical sequence; the components are listed by component number.

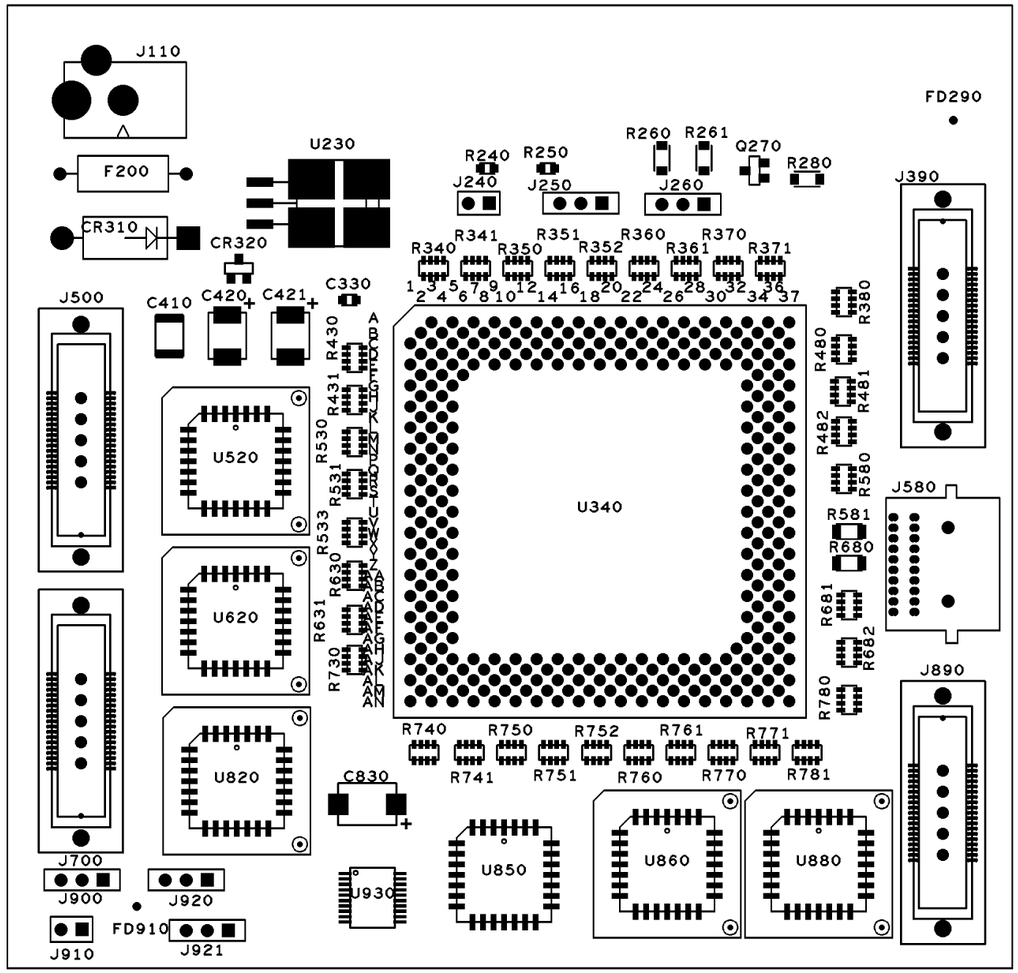


Component Locator Diagrams

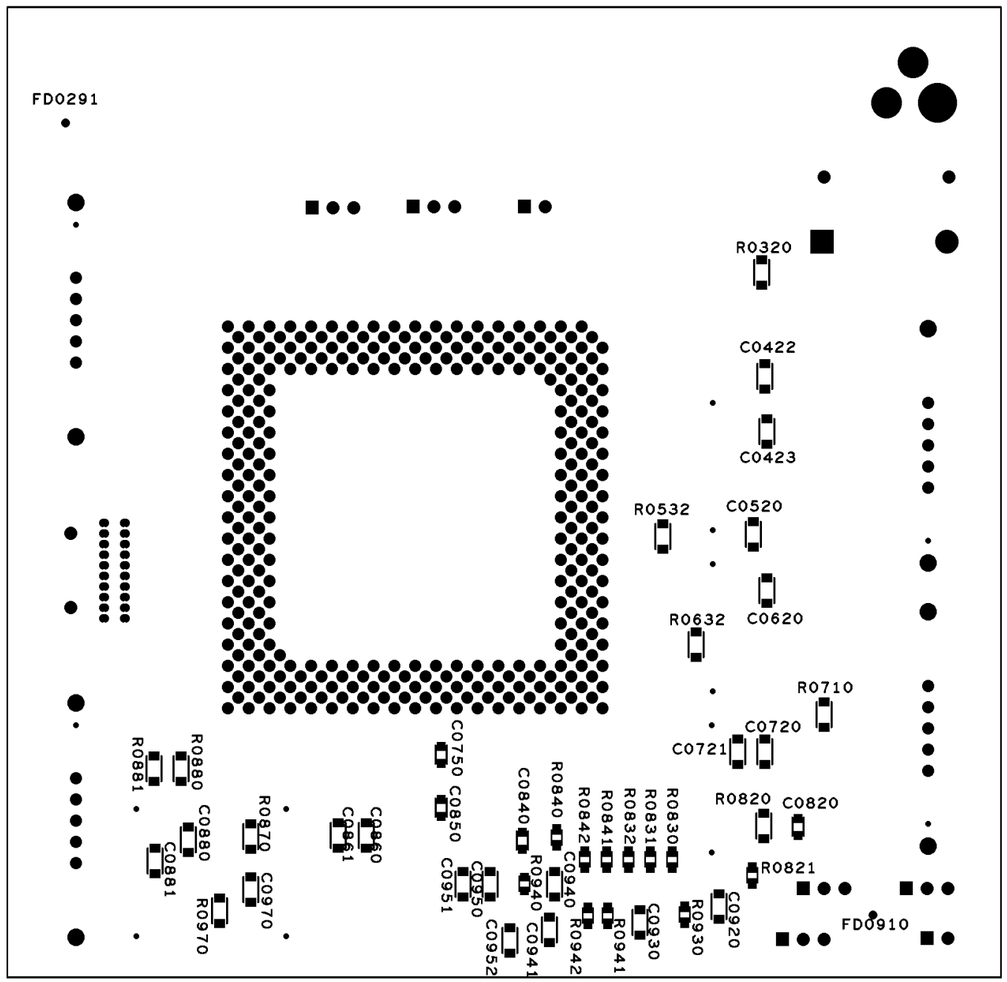
The schematic diagram and circuit board component location illustrations have grids marked on them. The component lookup tables refer to these grids to help you locate a component. The circuit board illustration appears only once; its lookup table lists the diagram number of all diagrams on which the circuitry appears.

Some of the circuit board component location illustrations are expanded and divided into several parts to make it easier for you to locate small components. To determine which part of the whole locator diagram you are looking at, refer to the small locator key shown below. The gray block, within the larger circuit board outline, shows where that part fits in the whole locator diagram. Each part in the key is labeled with an identifying letter that appears in the figure titles under component locator diagrams.



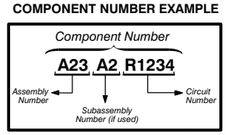


A1 Socket 7 Circuit Board (Front)



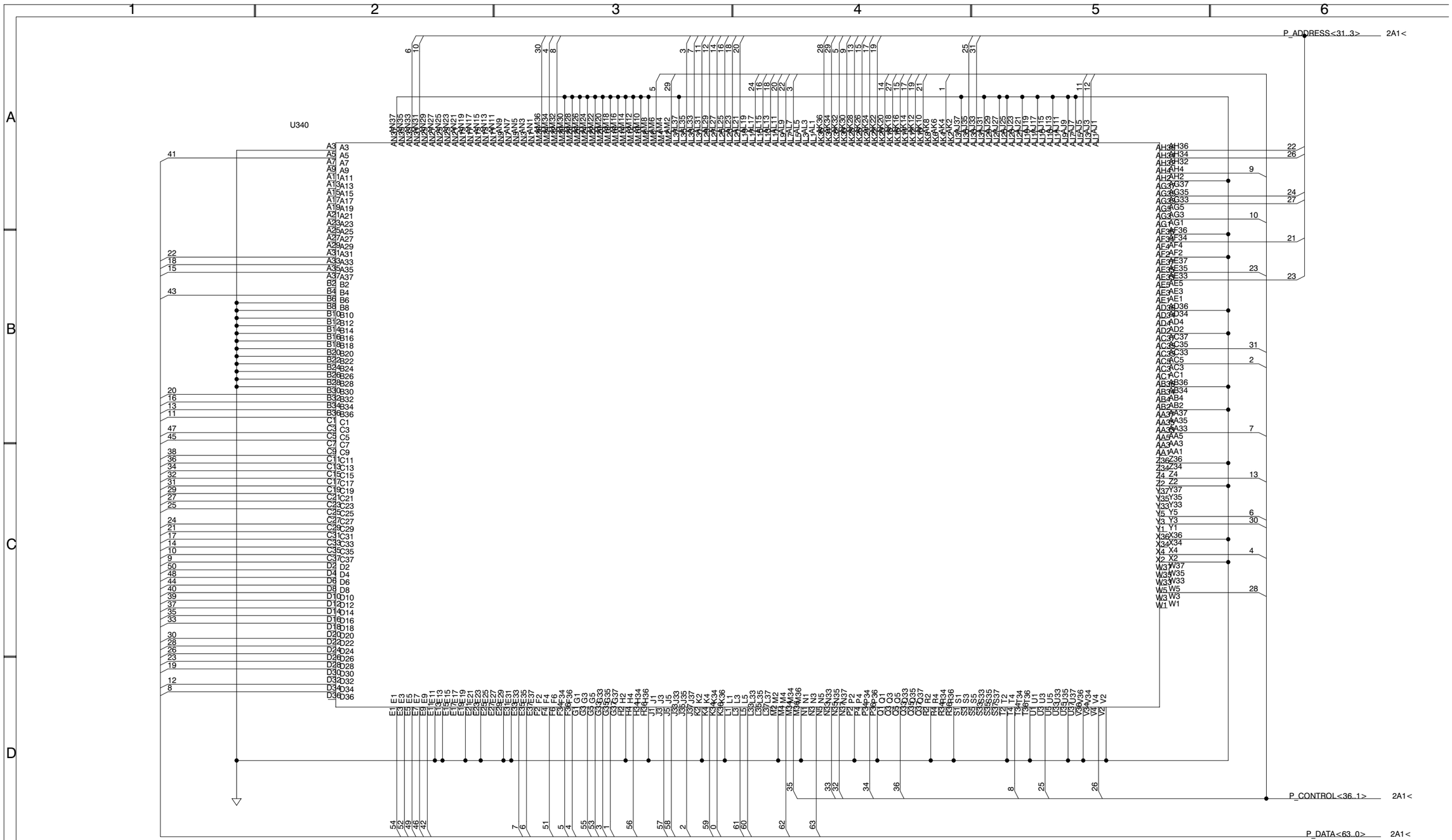
A1 Socket 7 Circuit Board (Back)

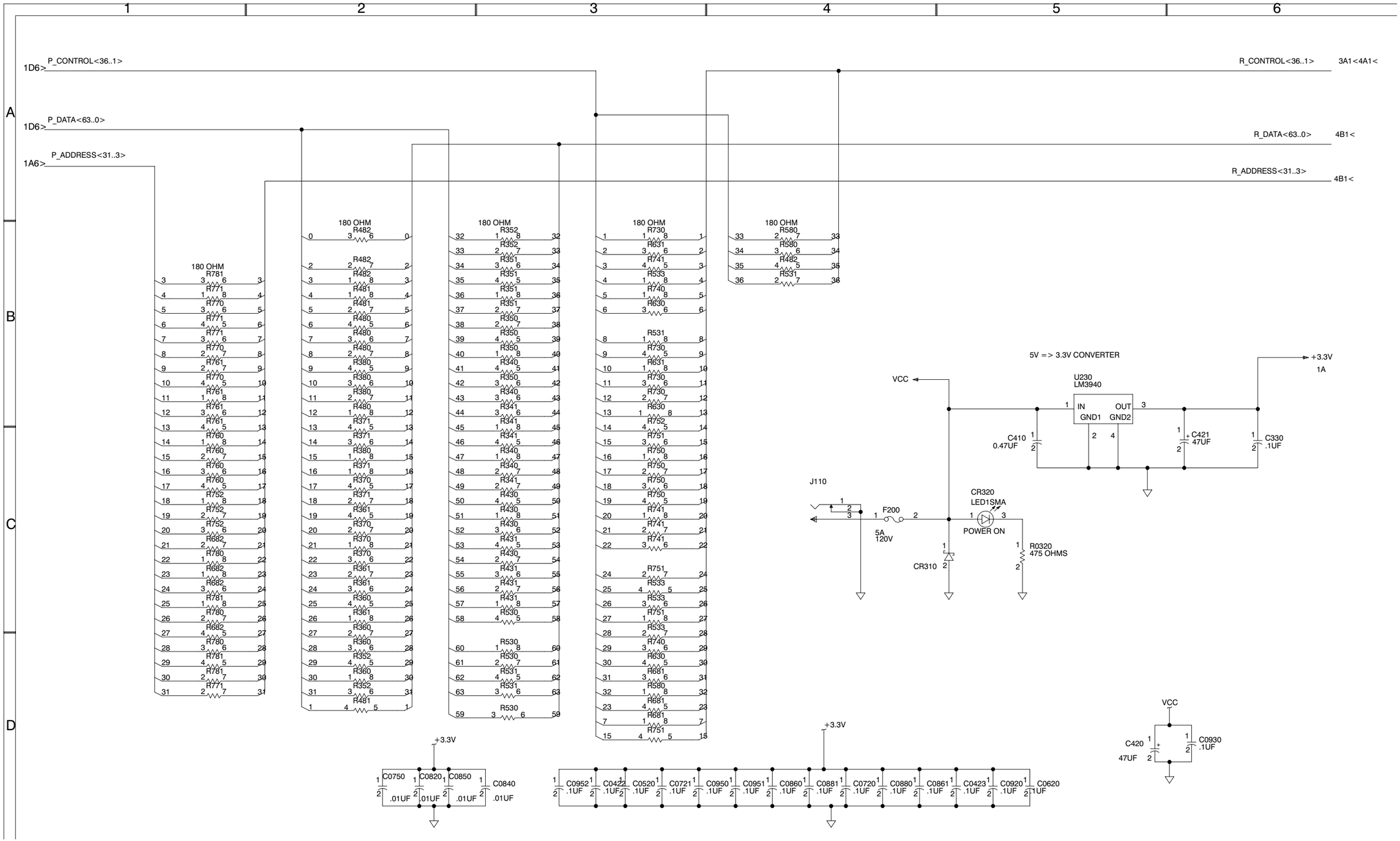
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

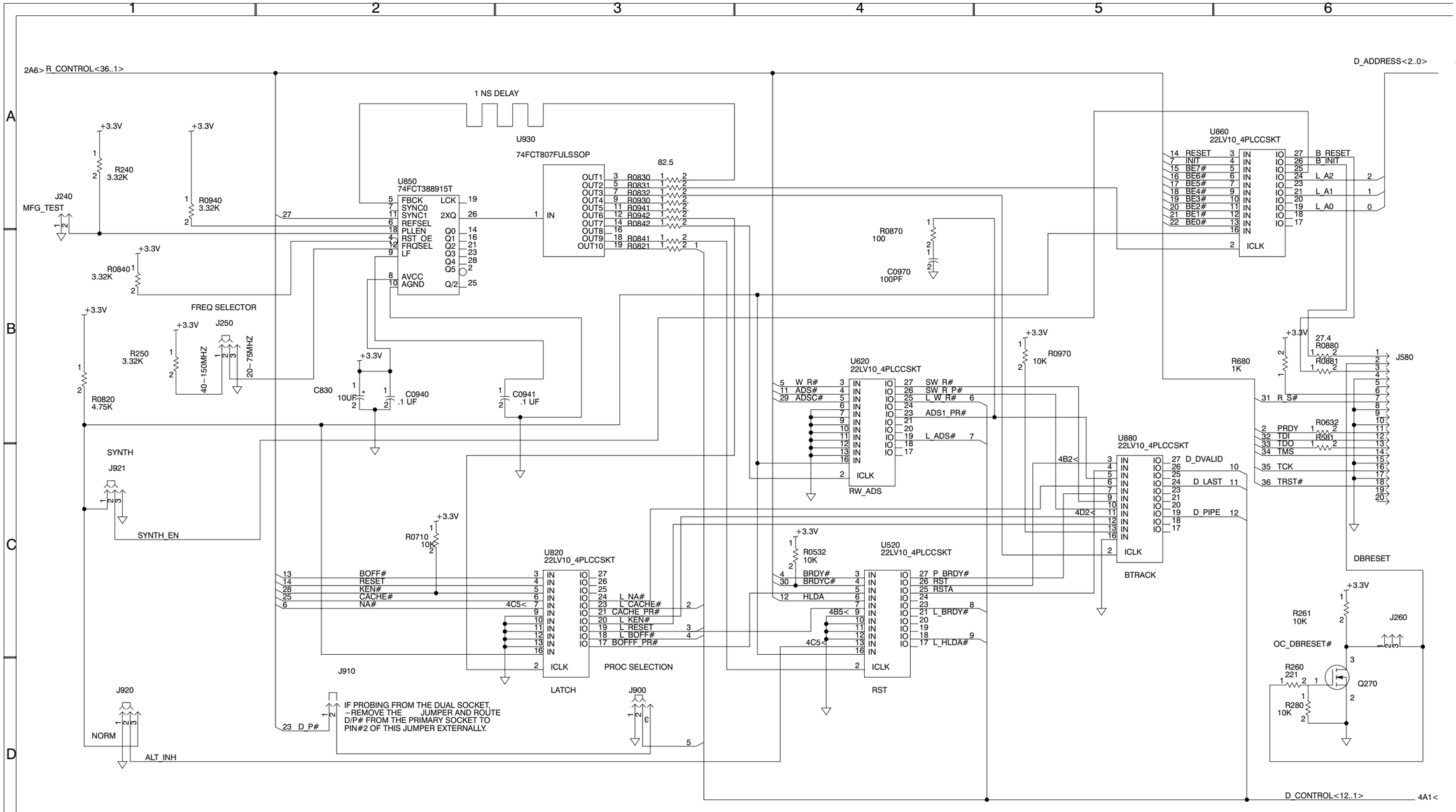
STATIC SENSITIVE DEVICES


U340
P_ADDRESS<31..3>
2A1<
P_CONTROL<36..1>
2A1<
P_DATA<63..0>
2A1<



TMS 109A Socket 7 Microprocessor Support

RES_PACK 1 A1 2


2A6> R_CONTROL<36..1>
D_ADDRESS<2..0>
4B1<
1 NS DELAY
U930
74FCT807FULSSOP
82.5
U850
74FCT388915T
FBCK
SYNC0
SYNC1
REFSEL
PLLEN
RST_OE
FRQSEL
LF
AVCC
AGND
LCK
2XQ
Q0
Q1
Q2
Q3
Q4
Q5
Q/2
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
R0830
R0831
R0832
R0930
R0941
R0942
R0842
R0841
R0821
IN
+3.3V
R240
3.32K
R0940
3.32K
J240
MFG_TEST
R0840
3.32K
FREQ SELECTOR
J250
R250
3.32K
40~150MHZ
20~75MHZ
R0820
4.75K
C830
10UF
C0940
.1 UF
C0941
.1 UF
R0870
100
C0970
100PF
U860
22LV10_4PLCCSKT
RESET
INIT
BE7#
BE6#
BE5#
BE4#
BE3#
BE2#
BE1#
BE0#
B_RESET
B_INIT
L_A2
L_A1
L_A0
ICLK
U620
22LV10_4PLCCSKT
W_R#
ADS#
ADSC#
SW_R#
SW_R_P#
L_W_R#
ADS1_PR#
L_ADS#
RW_ADS
R0970
10K
U880
22LV10_4PLCCSKT
D_DVALID
D_LAST
D_PIPE
BTRACK
R680
1K
27.4
R0880
R0881
J580
R_S#
R0632
R581
PRDY
TDI
TDO
TMS
TCK
TRST#
SYNTH
J921
SYNTH_EN
R0710
10K
U820
22LV10_4PLCCSKT
BOFF#
RESET
KEN#
CACHE#
NA#
L_NA#
L_CACHE#
CACHE_PR#
L_KEN#
L_RESET
L_BOFF#
BOFFF_PR#
LATCH
PROC SELECTION
J910
J920
NORM
ALT_INH
IF PROBING FROM THE DUAL SOCKET,
–REMOVE THE JUMPER AND ROUTE
D/P# FROM THE PRIMARY SOCKET TO
PIN#2 OF THIS JUMPER EXTERNALLY.
23 D_P#
J900
R0532
10K
BRDY#
BRDYC#
HLDA
U520
22LV10_4PLCCSKT
P_BRDY#
RST
RSTA
L_BRDY#
L_HLDA#
RST
DBRESET
R261
10K
J260
OC_DBRESET#
R260
221
Q270
R280
10K
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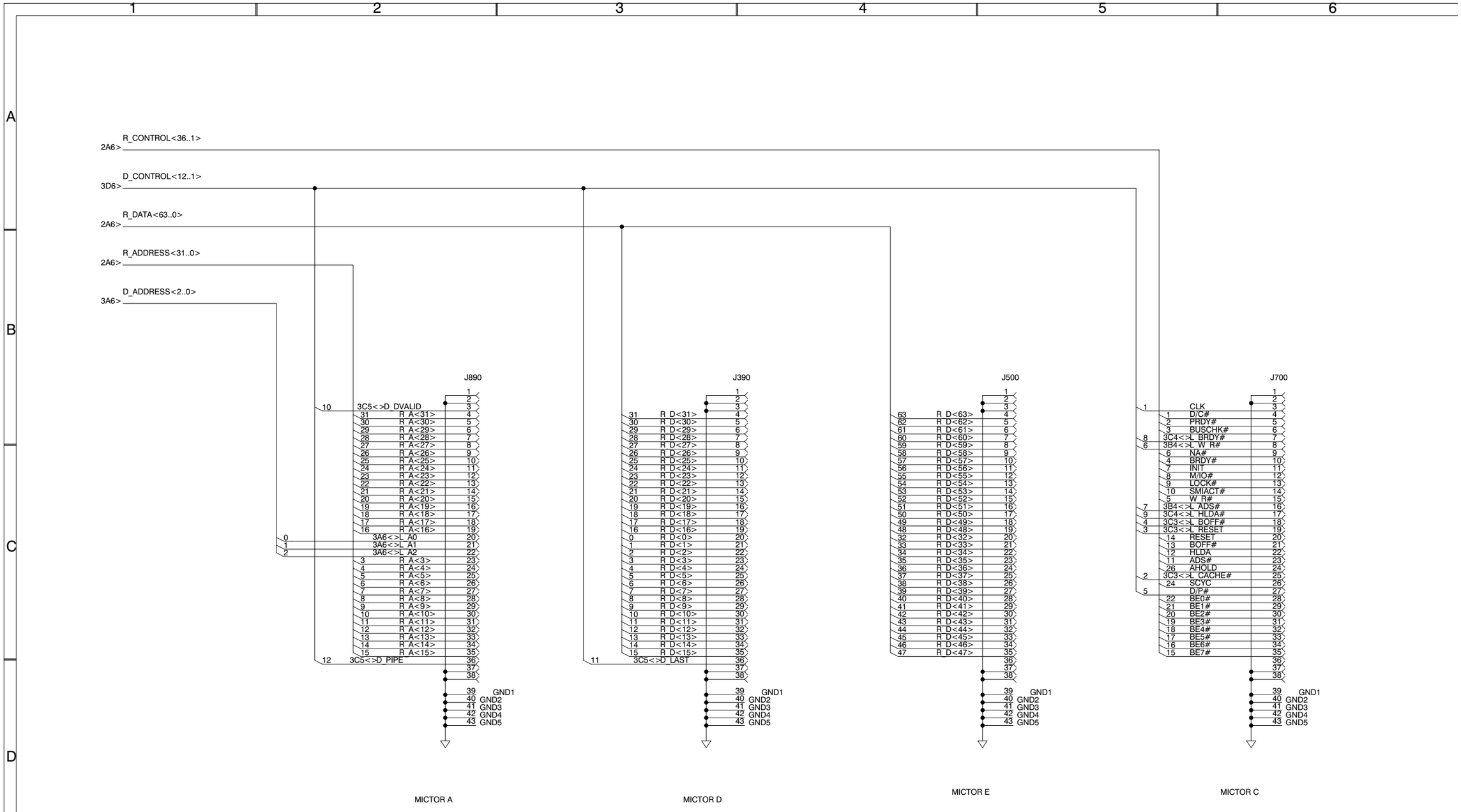
4B2<
4D2<
4C5<
4B5<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3
4
5
6
A
B
C
D
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2A6>
D_CONTROL<12..1>
3D6>
R_DATA<63..0>
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2A6>
D_ADDRESS<2..0>
3A6>
J890
10 3C5<>D_DVALID
31 R_A<31>
30 R_A<30>
29 R_A<29>
28 R_A<28>
27 R_A<27>
26 R_A<26>
25 R_A<25>
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21 R_A<21>
20 R_A<20>
19 R_A<19>
18 R_A<18>
17 R_A<17>
16 R_A<16>
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1 3A6<>L_A1
2 3A6<>L_A2
3 R_A<3>
4 R_A<4>
5 R_A<5>
6 R_A<6>
7 R_A<7>
8 R_A<8>
9 R_A<9>
10 R_A<10>
11 R_A<11>
12 R_A<12>
13 R_A<13>
14 R_A<14>
15 R_A<15>
12 3C5<>D_PIPE
39 GND1
40 GND2
41 GND3
42 GND4
43 GND5
MICTOR A
J390
31 R_D<31>
30 R_D<30>
29 R_D<29>
28 R_D<28>
27 R_D<27>
26 R_D<26>
25 R_D<25>
24 R_D<24>
23 R_D<23>
22 R_D<22>
21 R_D<21>
20 R_D<20>
19 R_D<19>
18 R_D<18>
17 R_D<17>
16 R_D<16>
0 R_D<0>
1 R_D<1>
2 R_D<2>
3 R_D<3>
4 R_D<4>
5 R_D<5>
6 R_D<6>
7 R_D<7>
8 R_D<8>
9 R_D<9>
10 R_D<10>
11 R_D<11>
12 R_D<12>
13 R_D<13>
14 R_D<14>
15 R_D<15>
11 3C5<>D_LAST
39 GND1
40 GND2
41 GND3
42 GND4
43 GND5
MICTOR D
J500
63 R_D<63>
62 R_D<62>
61 R_D<61>
60 R_D<60>
59 R_D<59>
58 R_D<58>
57 R_D<57>
56 R_D<56>
55 R_D<55>
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36 R_D<36>
37 R_D<37>
38 R_D<38>
39 R_D<39>
40 R_D<40>
41 R_D<41>
42 R_D<42>
43 R_D<43>
44 R_D<44>
45 R_D<45>
46 R_D<46>
47 R_D<47>
39 GND1
40 GND2
41 GND3
42 GND4
43 GND5
MICTOR E
J700
1 CLK
1 D/C#
2 PRDY#
3 BUSCHK#
8 3C4<>L_BRDY#
6 3B4<>L_W_R#
6 NA#
4 BRDY#
7 INIT
8 M/IO#
9 LOCK#
10 SMIACT#
5 W_R#
7 3B4<>L_ADS#
9 3C4<>L_HLDA#
4 3C3<>L_BOFF#
3 3C3<>L_RESET
14 RESET
13 BOFF#
12 HLDA
11 ADS#
26 AHOLD
2 3C3<>L_CACHE#
24 SCYC
5 D/P#
22 BE0#
21 BE1#
20 BE2#
19 BE3#
18 BE4#
17 BE5#
16 BE6#
15 BE7#
39 GND1
40 GND2
41 GND3
42 GND4
43 GND5
MICTOR C

Replaceable Parts

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 109A Socket 7 microprocessor support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
01KV9	MERIX CORP	1521 POPLAR LANE PO BOX 3000	FOREST GROVE, OR 97116
04713	MOTOROLA INC	SEMICONDUCTOR PRODUCTS SECTOR 5005 E MCDOWELL ROAD	PHOENIX, AZ 85008–4229
22526	BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319–9769
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	BERG ELECTRONICS INC.	MCKENZIE SOCKET DIV 910 PAGE AVE	FREMONT, CA 94538–7340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
82389	SWITCHCRAFT	DIV OF RAYTHEON 5555 N. ELSTON AVENUE	CHICAGO, IL 60630–1314
85480	BRADY USA	NAMEPLATE DIVISION P O BOX 571 346 ELIZABETH BRADY RD	HILLSBOROUGH, NC 27278

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6–1–0	010–0614–00			1	ADAPTER,PROBE SOCKET–7, SOCKETED, PGA–321 PIN;TMS109A	80009	010–0614–00
–1	671–4737–00			1	CIRCUIT BOARD:SOCKET–7,SOCKETED,PGA–321 PIN,TMS109A	80009	671–4737–00
–2	105–1089–00			4	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105–1089–00
–3	131–6134–01			4	CONN,RCPT:SMD,MICTOR,FEMALE,STR,38 POS,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLADIUM	00779	767054–1
–4	131–4406–00			1	CONN,HDR:PCB,MALE,RTANG,2 X 10,0.05 X 0.1 CTR,0.350 H X 0.100 TAIL,CTR PLZ,LATCHING,30 G	00779	104069–1
–5	131–1857–00			1	CONN,HDR:PCB,MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD,	22526	65507–136
–6	136–1342–00			1	SOCKET (AMD) ,PGA:PCB,PGA,STR,321 POS,37 X 37, OPEN CTR,SHORT PINS, 0.1 X 0.1 CTR, 30 GOLD	63058	PZA–321H–120B–37AU
–7	136–1346–00			1	SOCKET (INTEL) ,PGA:PCB,STR,296 POS,36X36, OPEN CTR,0.10 X 0.10 CTR,0.165 H X 0.125 TAIL, 30	63058	PZA–63150–001
–8	131–6610–00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM D PIN,BRASS,SILVER PLATE,5A,	82389	RAPC722TB
–9	159–0059–00			1	FUSE,WIRE LEAD:5A,125V	61857	SPI–5A
–10	131–4917–00			1	CONN,HDR:PCB,MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30 GOLD,TUBE,HIGH TEMP,	00779	104350–1
–11	131–4530–00			5	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
–12	131–4356–00			5	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,30 GOLD,	26742	9618–302–50
					STANDARD ACCESSORIES		
	071–0497–01			1	MANUAL,TECH:INSTRUCTION, SOCKET–7; TMS109A	80009	071–0497–01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH,RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63 HZ IEC,15X8.6X5 CM, UL,CSA, TUV,IEC,SELF	14310	SW108KA0002F01
					OPTIONAL ACCESSORIES		
	———————*			4	P6434 MASS TERMINATION PROBE, Opt 21 *	80009	P6434
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,AUSTRALIA,SAFTEY CONTROLLED,	TK1373	161–0104–05
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,EUROPEAN,SAFTEY CONTROLLED	TK1373	ORDER BY DESCRIPTION

Replaceable parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG,IEC320,RCPT X 13A,FUSED,UK PLUG,(13A FUSE)	TK2541	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,SWISS,NO CORD GRIP,SAFTEY CONTR	S3109	ORDER BY DESCRIPTION

*** Check the P6434 manual for detailed replaceable part number information.**

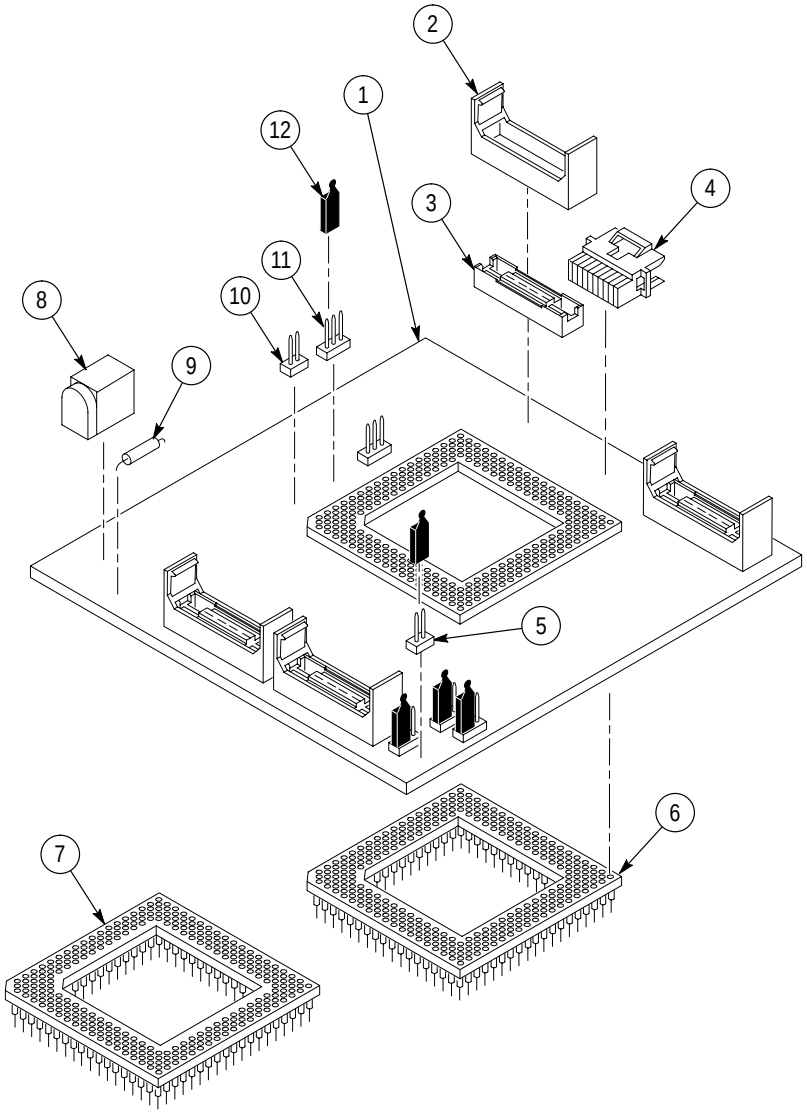

Figure 6–1: TMS 109A Socket 7 probe adapter exploded view

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